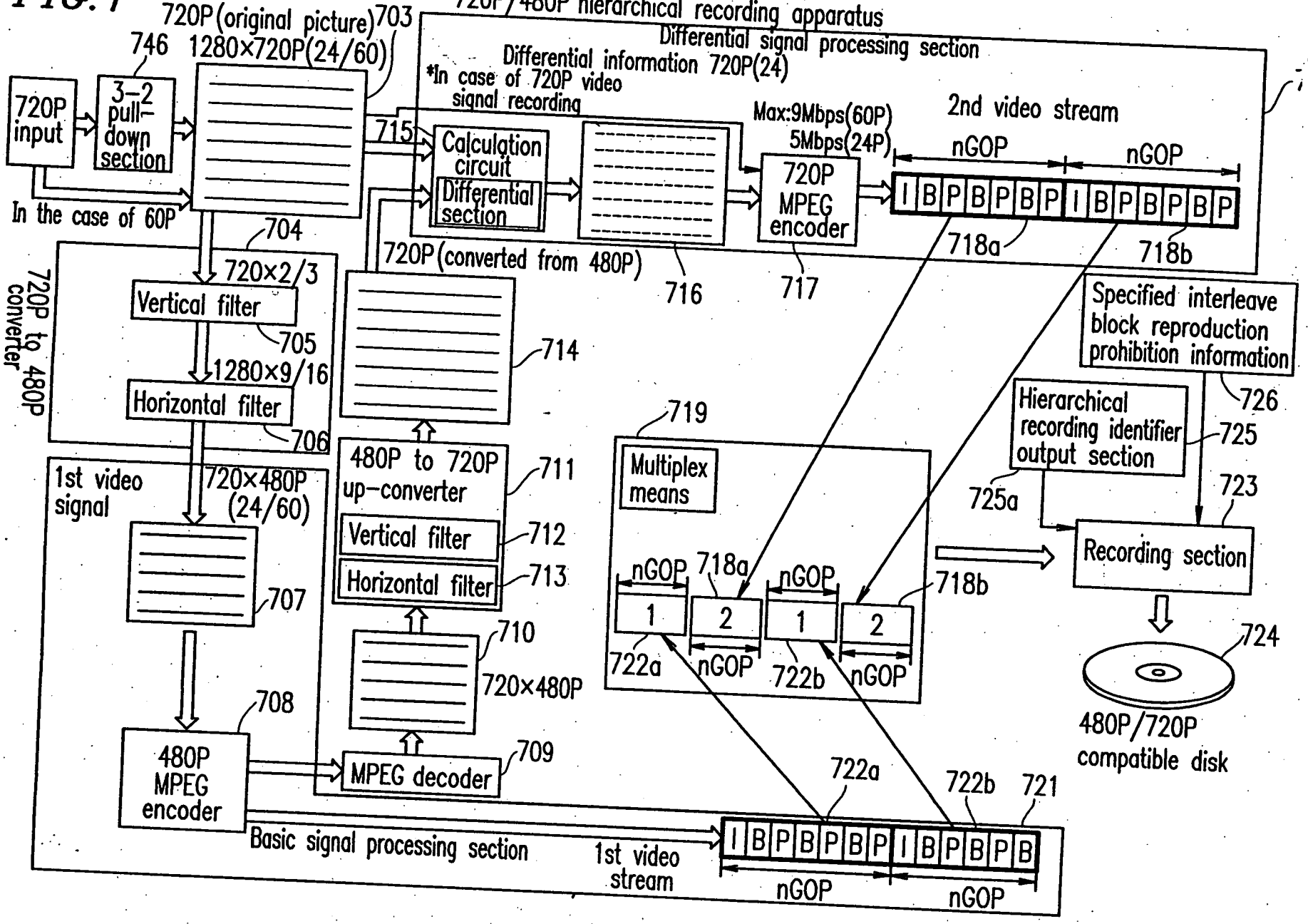
FIG. 1



1/60

09/486538

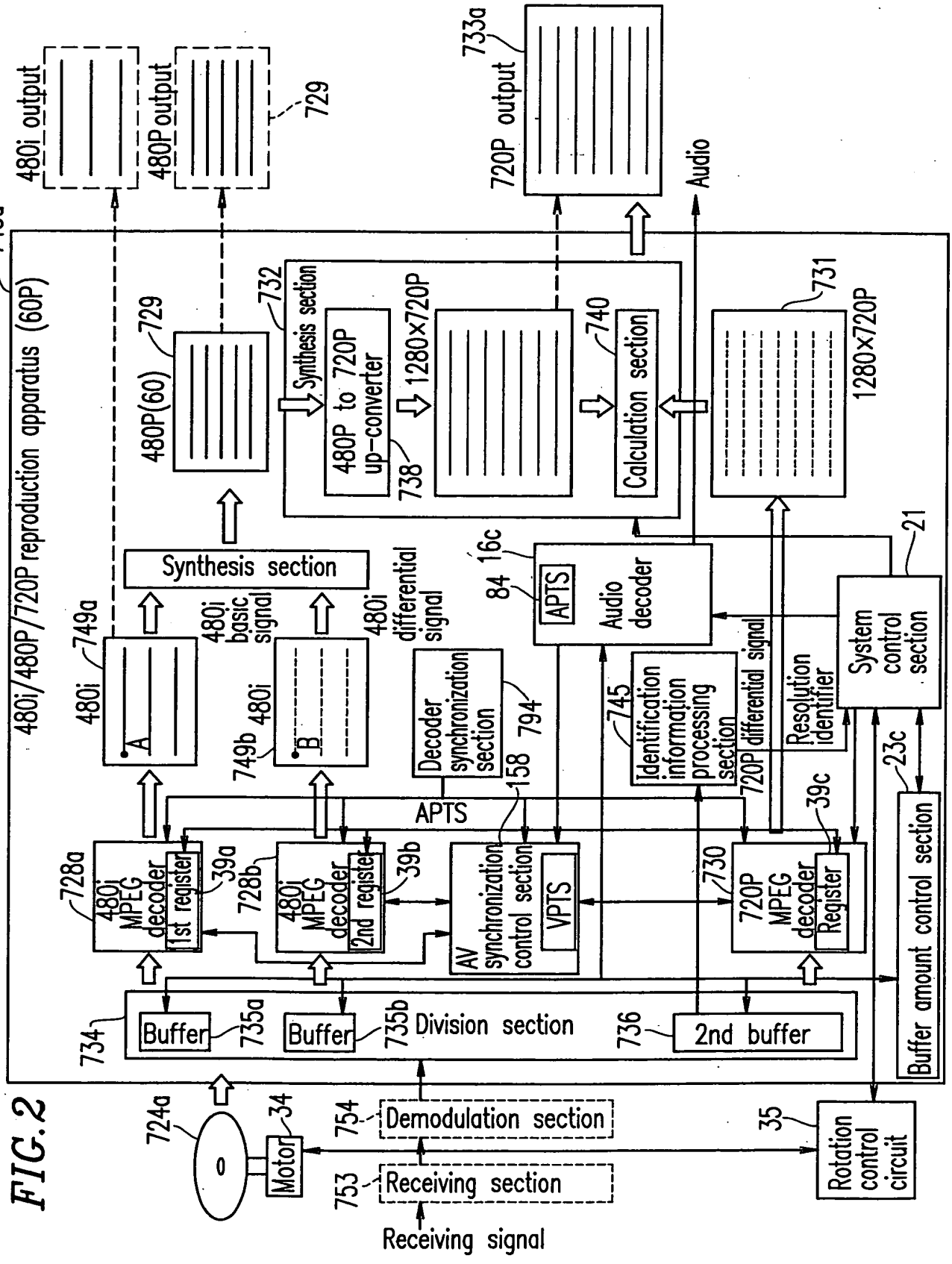

743a
480i/480P/720P reproduction apparatus (60P)
480i output
480P output
729
733a
720P output
Audio
731
1280×720P
732
Synthesis section
480P to 720P up-converter
738
1280×720P
740
Calculation section
480P(60)
729
Synthesis section
480i basic signal
480i differential signal
749a
480i
A
749b
480i
B
16c
84
APTS
Audio decoder
21
System control section
Decoder synchronization section
794
158
745
Identification information processing section
720P differential signal
Resolution identifier
APTS
39c
23c
728a
480i MPEG decoder
1st register
39a
728b
480i MPEG decoder
2nd register
39b
AV synchronization control section
VPTS
730
720P MPEG decoder
Register
Buffer amount control section
734
Buffer
735a
Buffer
735b
Division section
736
2nd buffer
724a
34
Motor
754
Demodulation section
753
Receiving section
Receiving signal
35
Rotation control circuit

FIG.2

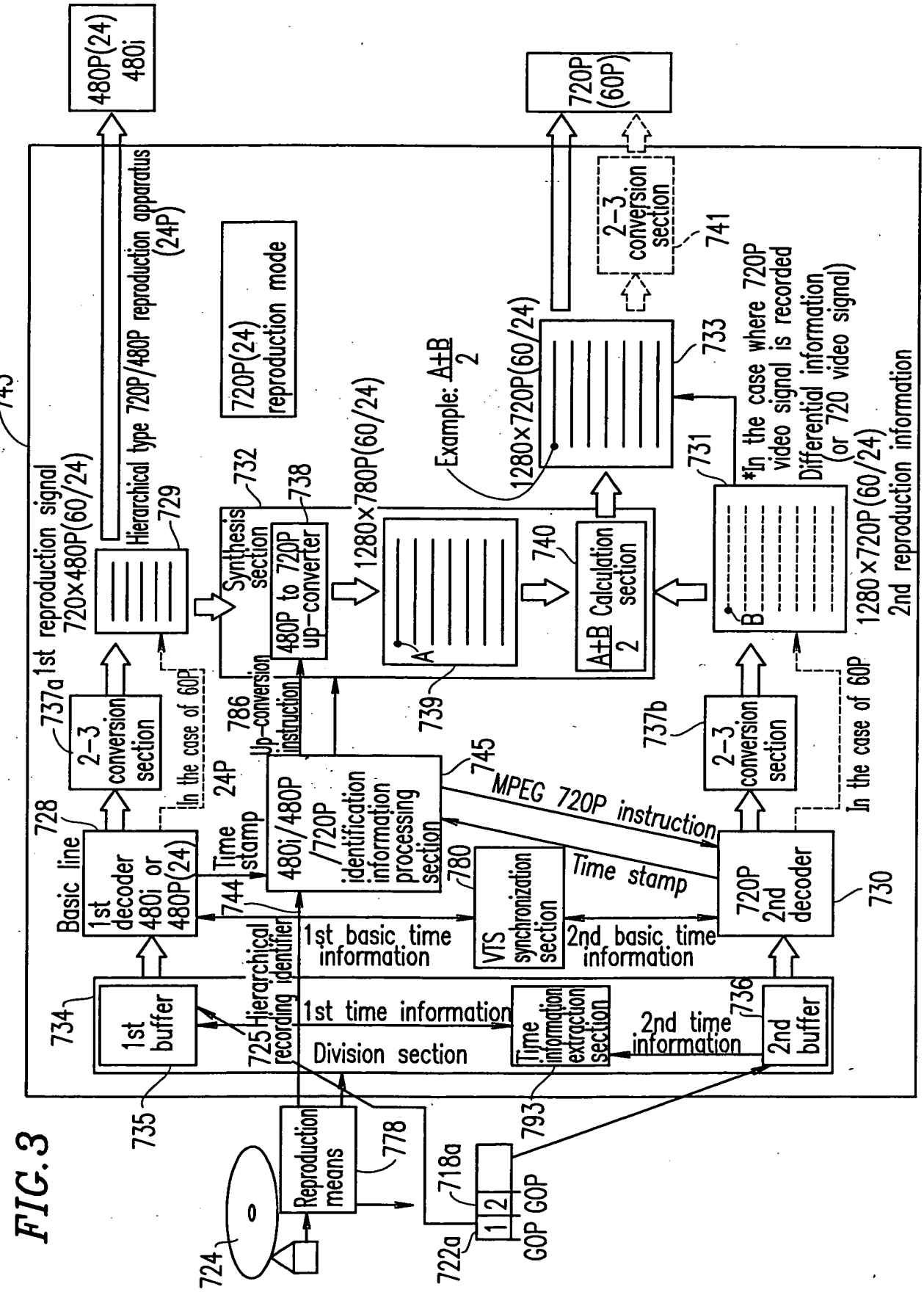

480P(24)
480i
720P
(60P)
743
Hierarchical type 720P/480P reproduction apparatus
(24P)
720P(24)
reproduction mode
2-3
conversion
section
741
1st reproduction signal
720×480P(60/24)
729
732
Synthesis
section
738
480P to 720P
up-converter
1280×780P(60/24)
Example: A+B/2
1280×720P(60/24)
733
731
*In the case where 720P
video signal is recorded
Differential information
(or 720 video signal)
1280×720P(60/24)
2nd reproduction information
737a
2-3
conversion
section
In the case of 60P
786
Up-conversion
instruction
739
740
A+B
2
Calculation
section
B
737b
2-3
conversion
section
In the case of 60P
728
Basic line
1st
decoder
480i or
480P(24)
24P
Time
stamp
744
480i/480P
/720P
identification
information
processing
section
745
MPEG 720P instruction
780
VTS
synchronization
section
Time stamp
720P
2nd
decoder
730
Hierarchical
recording identifier
1st basic time
information
2nd basic time
information
734
1st
buffer
725
1st time information
Division section
Time
information
extraction
section
2nd time
information
736
2nd
buffer
735
793
Reproduction
means
778
718a
724
722a
1
2
GOP
GOP

FIG. 3

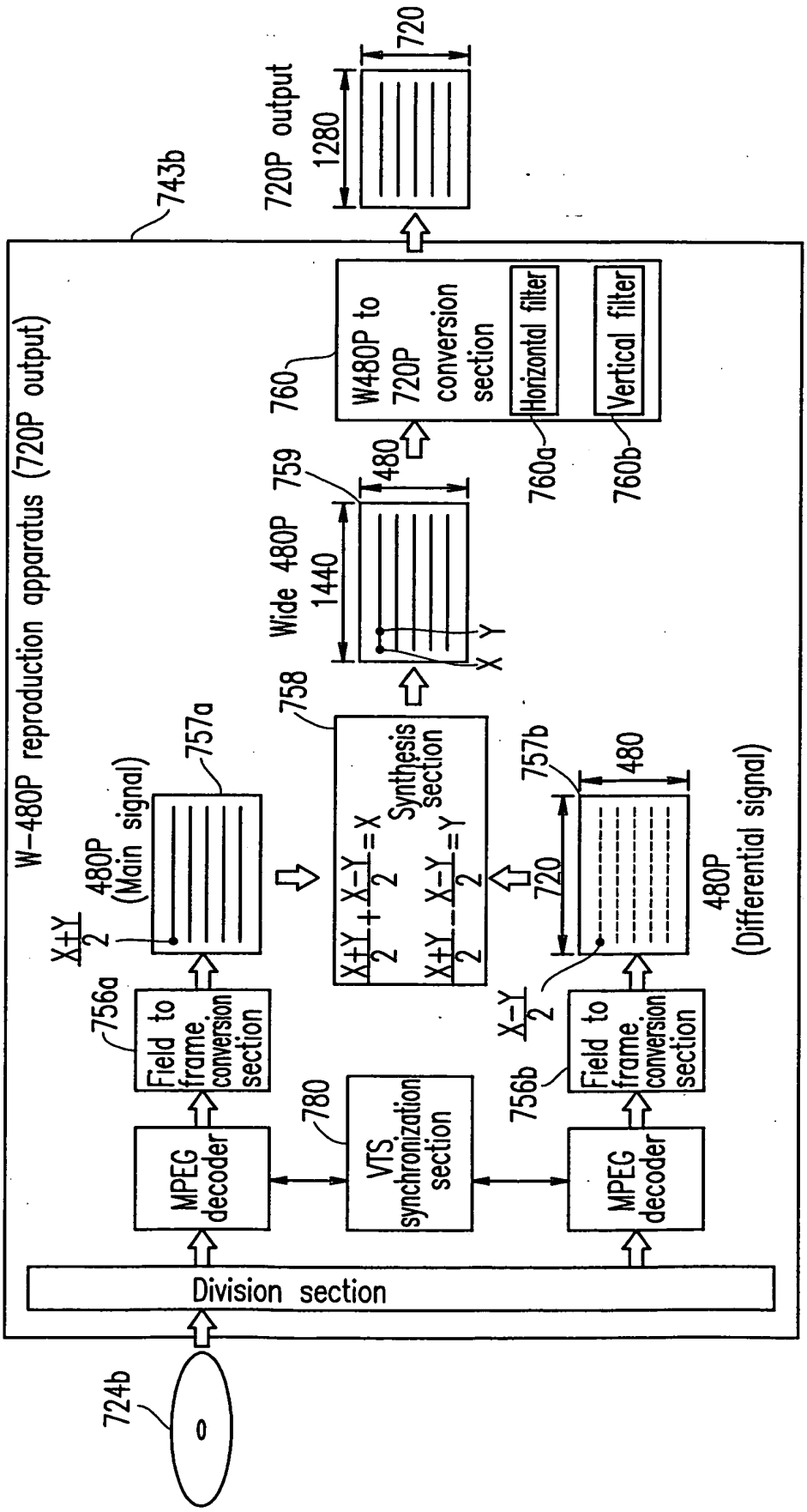

724b
0
Division section
W-480P reproduction apparatus (720P output)
743b
MPEG decoder
Field to frame conversion section
756a
480P (Main signal)
757a
X+Y/2
780
VTS synchronization section
MPEG decoder
Field to frame conversion section
756b
X-Y/2
757b
480
720
480P (Differential signal)
X+Y/2 + X-Y/2 = X
X+Y/2 - X-Y/2 = Y
758
Synthesis section
Wide 480P
1440
759
480
X
Y
W480P to 720P conversion section
760
Horizontal filter
760a
Vertical filter
760b
720P output
1280
720

FIG. 4

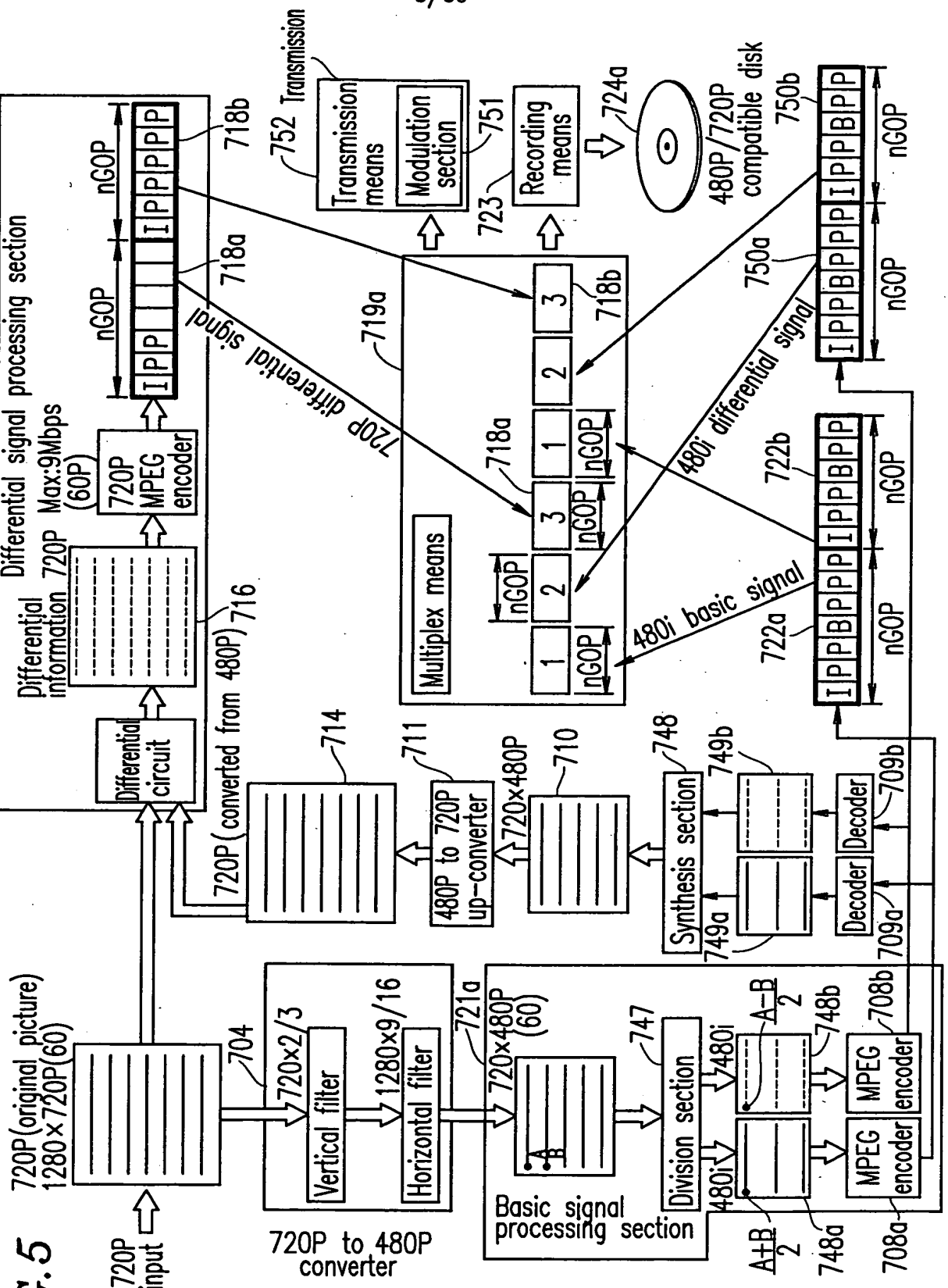

720P input
720P(original picture) 1280×720P(60)
704
720×2/3
Vertical filter
1280×9/16
Horizontal filter
721a
720P to 480P converter
720×480P (60)
747
Division section
480i
480i
A+B 2
A−B 2
748a
748b
Basic signal processing section
MPEG encoder
MPEG encoder
708a
708b
720P(converted from 480P)
714
480P to 720P up-converter
711
720×480P
710
Synthesis section
748
749a
749b
Decoder
Decoder
709a
709b
720P/480P/480i hierarchical recording apparatus
Differential signal processing section
Differential circuit
Differential information 720P
716
720P MPEG encoder
Max:9Mbps (60P)
nGOP
718a
718b
720P differential signal
719a
Multiplex means
480i basic signal
480i differential signal
722a
722b
750a
750b
480P/720P compatible disk
724a
Recording means
723
Modulation section
751
Transmission means
752 Transmission

FIG. 5

FIG. 6

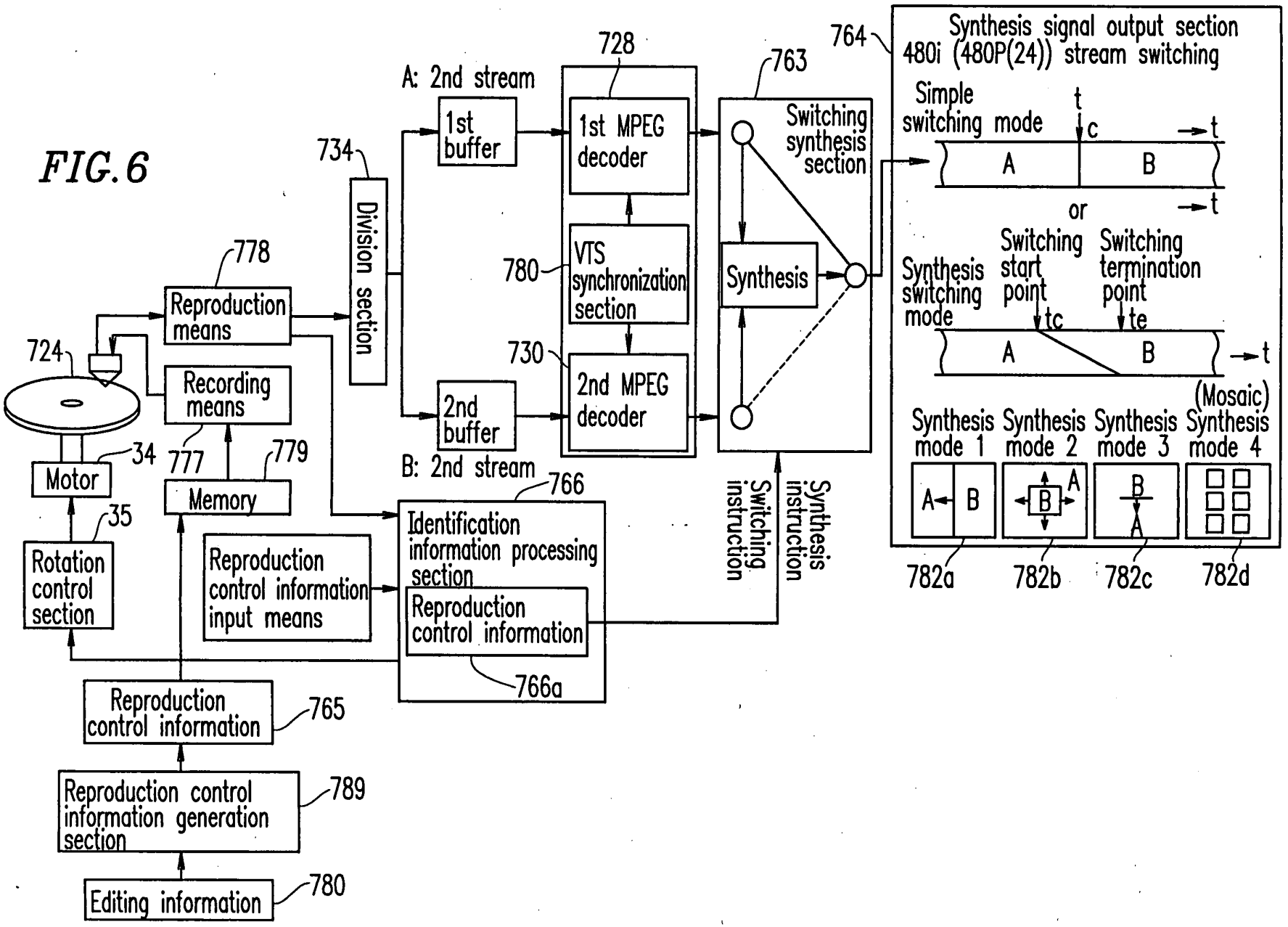
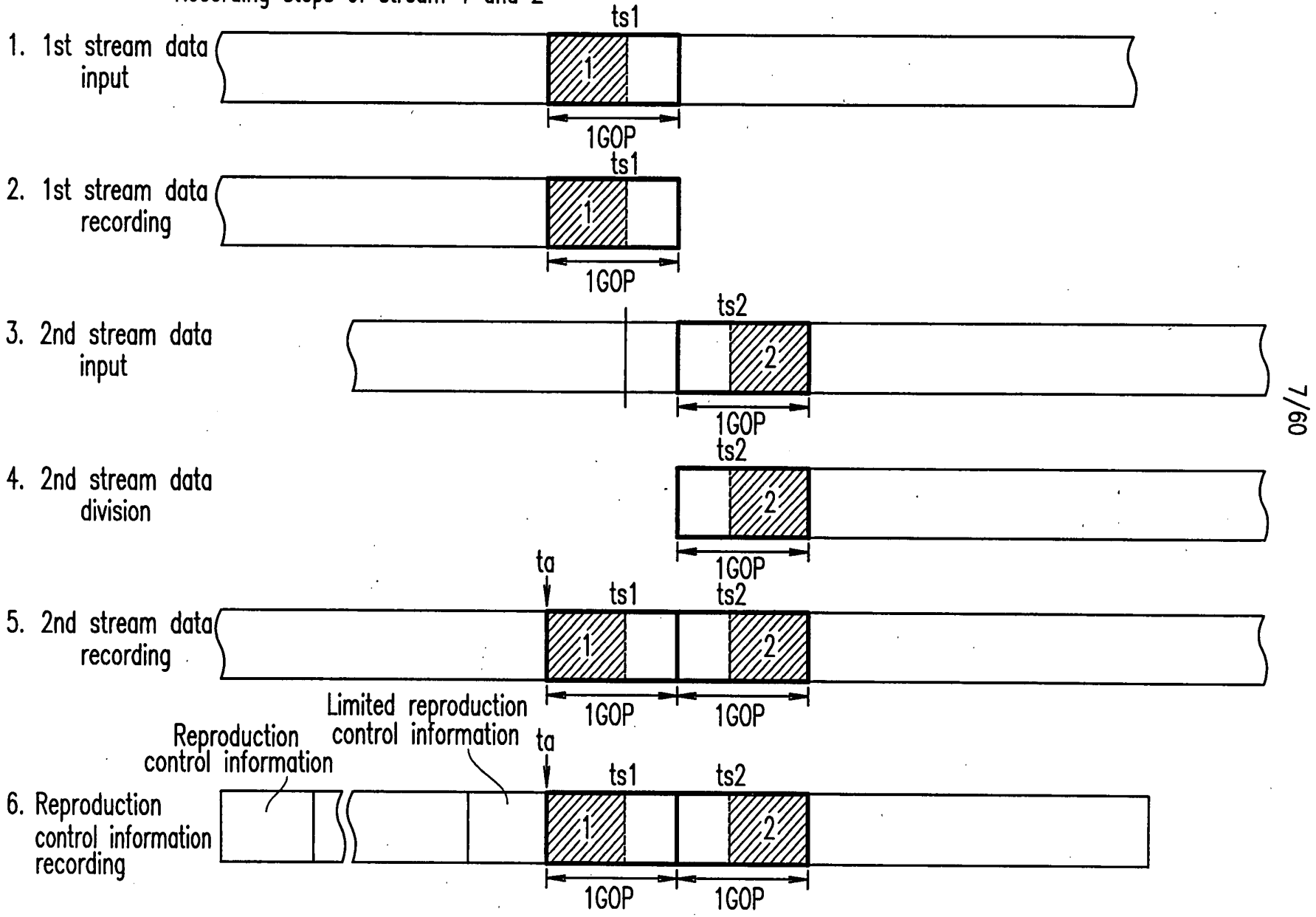

Synthesis signal output section
480i (480P(24)) stream switching
764
Simple switching mode
t
c
A
B
or
Synthesis switching mode
Switching start point
tc
Switching termination point
te
(Mosaic)
Synthesis mode 1
Synthesis mode 2
Synthesis mode 3
Synthesis mode 4
782a
782b
782c
782d
728
763
Switching synthesis section
Synthesis
1st MPEG decoder
2nd MPEG decoder
VTS synchronization section
780
730
A: 2nd stream
B: 2nd stream
1st buffer
2nd buffer
734
Division section
778
Reproduction means
Recording means
777
779
Memory
724
Motor
34
35
Rotation control section
Reproduction control information input means
766
Identification information processing section
Reproduction control information
766a
Switching instruction
Synthesis instruction
Reproduction control information
765
Reproduction control information generation section
789
Editing information
780

FIG. 7



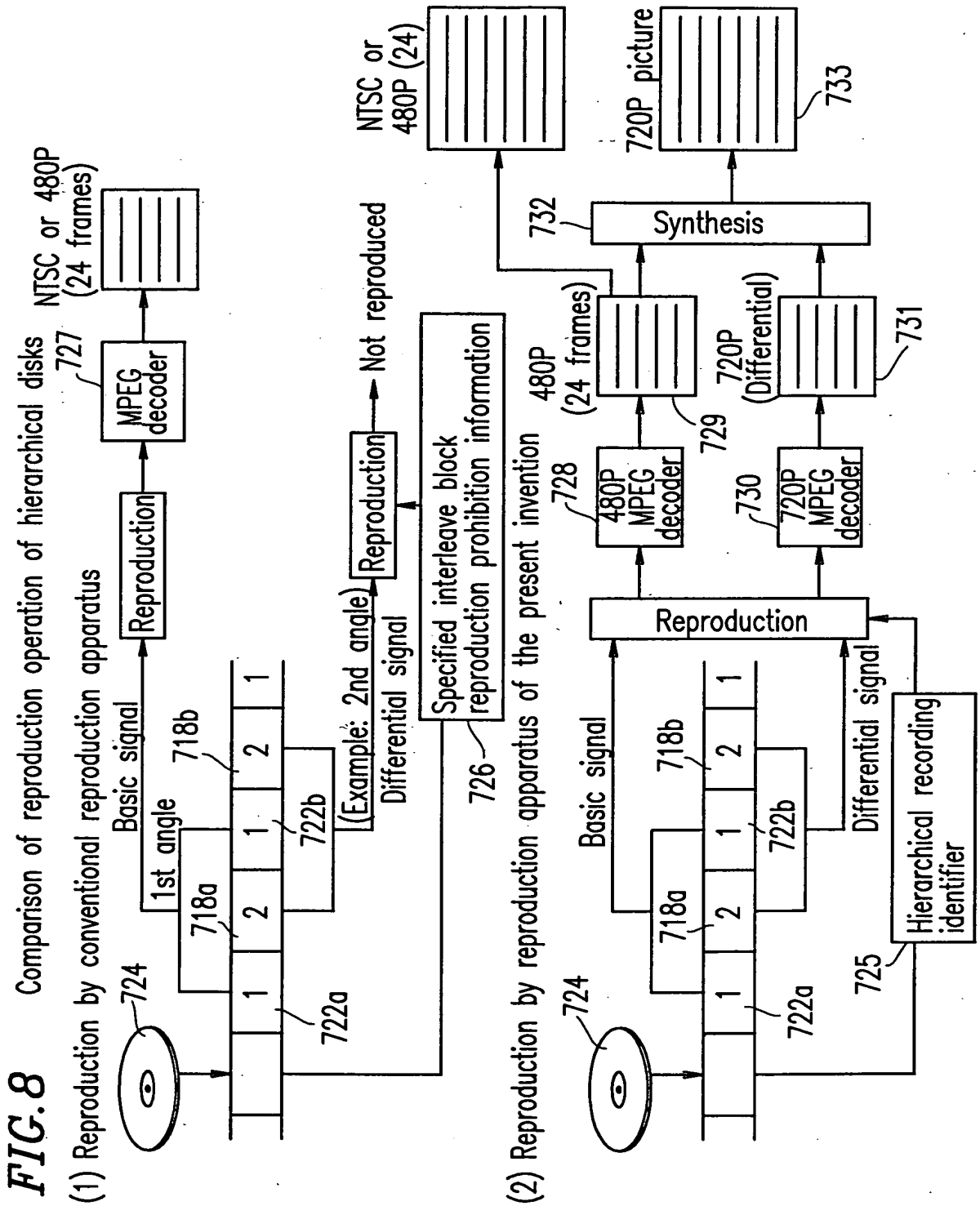
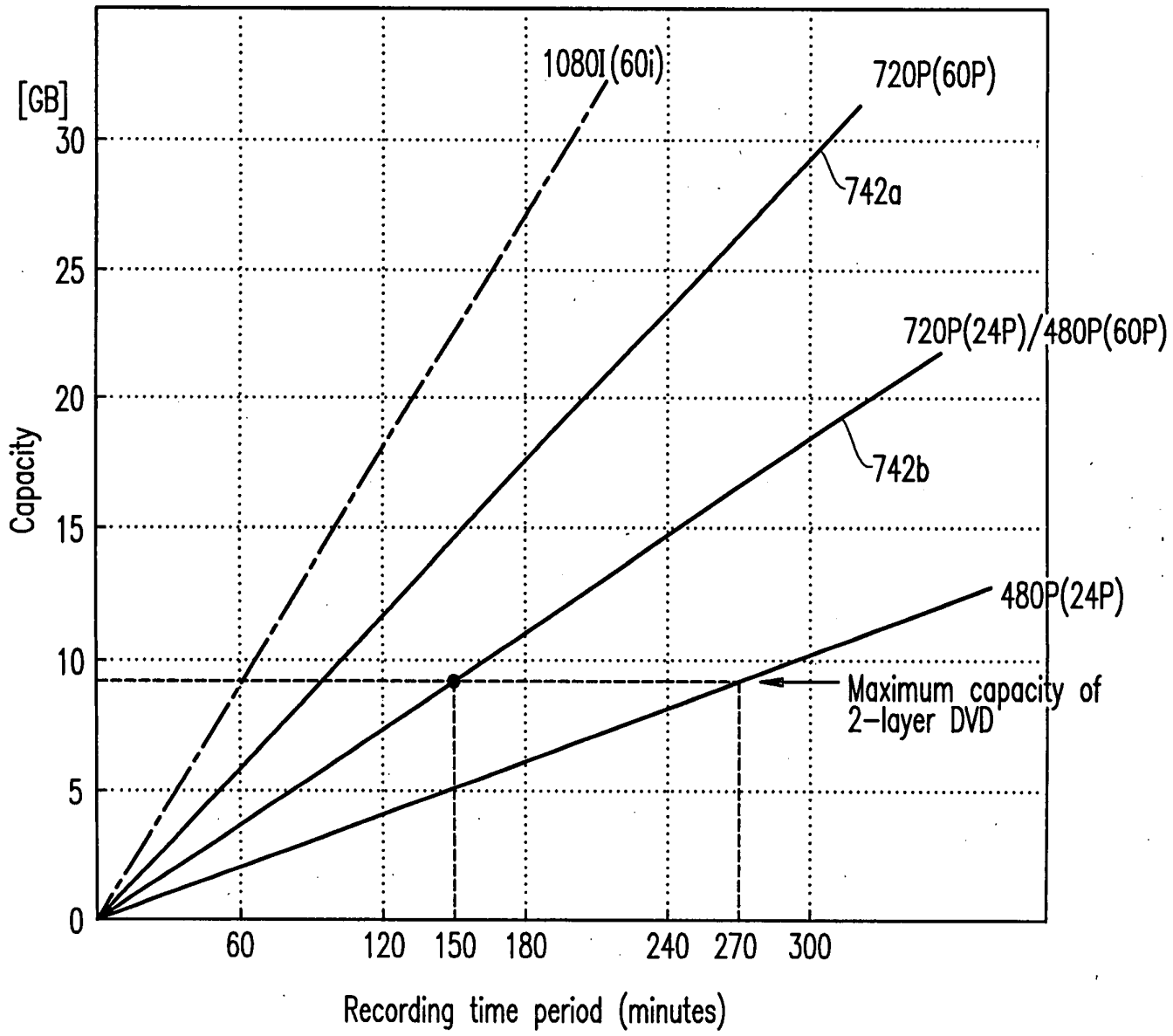


FIG. 8 Comparison of reproduction operation of hierarchical disks

FIG. 9



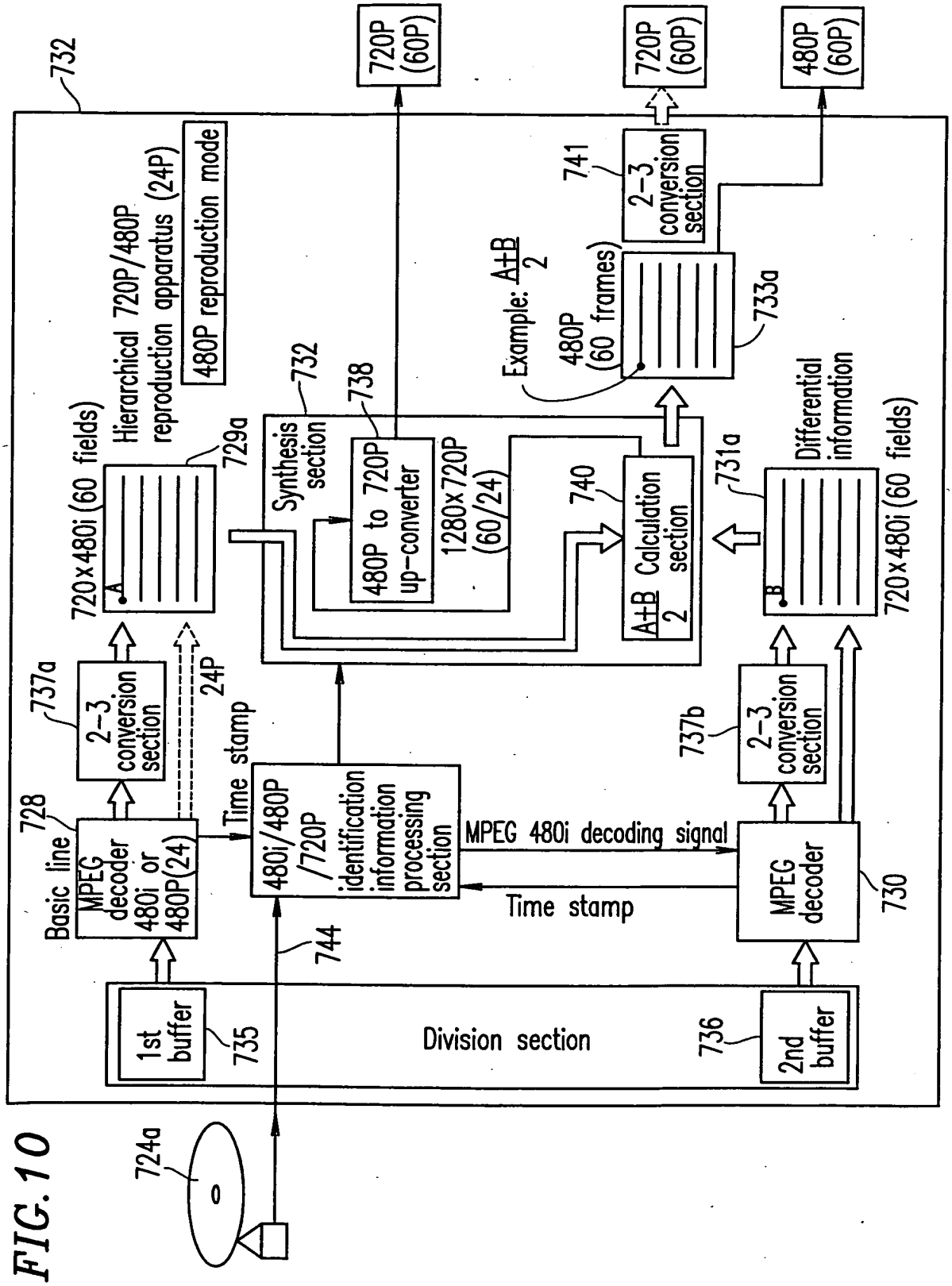

732
720P (60P)
720P (60P)
480P (60P)
741
2-3 conversion section
Example: A+B / 2
480P (60 frames)
733a
Hierarchical 720P/480P reproduction apparatus (24P)
480P reproduction mode
720x480i (60 fields)
729a
Synthesis section
738
480P to 720P up-converter
1280x720P (60/24)
740
A+B / 2 Calculation section
731a
Differential information
720x480i (60 fields)
737a
2-3 conversion section
24P
Time stamp
737b
2-3 conversion section
728
Basic line MPEG decoder 480i or 480P(24)
480i/480P /720P identification information processing section
MPEG 480i decoding signal
Time stamp
MPEG decoder
730
744
1st buffer
735
Division section
736
2nd buffer
724a

FIG. 10

FIG. 11 Reproduction control information

766 Switching point number S	767 Picture synthesis identifier	1st stream 768 Switching start address:ts1	1st stream 769 Switching termination address:te2	2nd stream 770 GOP start address:tsG	2nd stream 771 Switching start address:ts2	2nd stream 772 Switching termination address:te2	2nd stream 773 Decoding start address:ta
1	None	ts1-1		tsG-1	ts2-1		ta1
2	Mode 1	ts1-2	te2-2	tsG-2	ts2-2	te2-2	ta2
3	Mode 2	ts1-3	te2-3	tsG-3	ts2-3	te2-3	ta3

765

FIG. 12

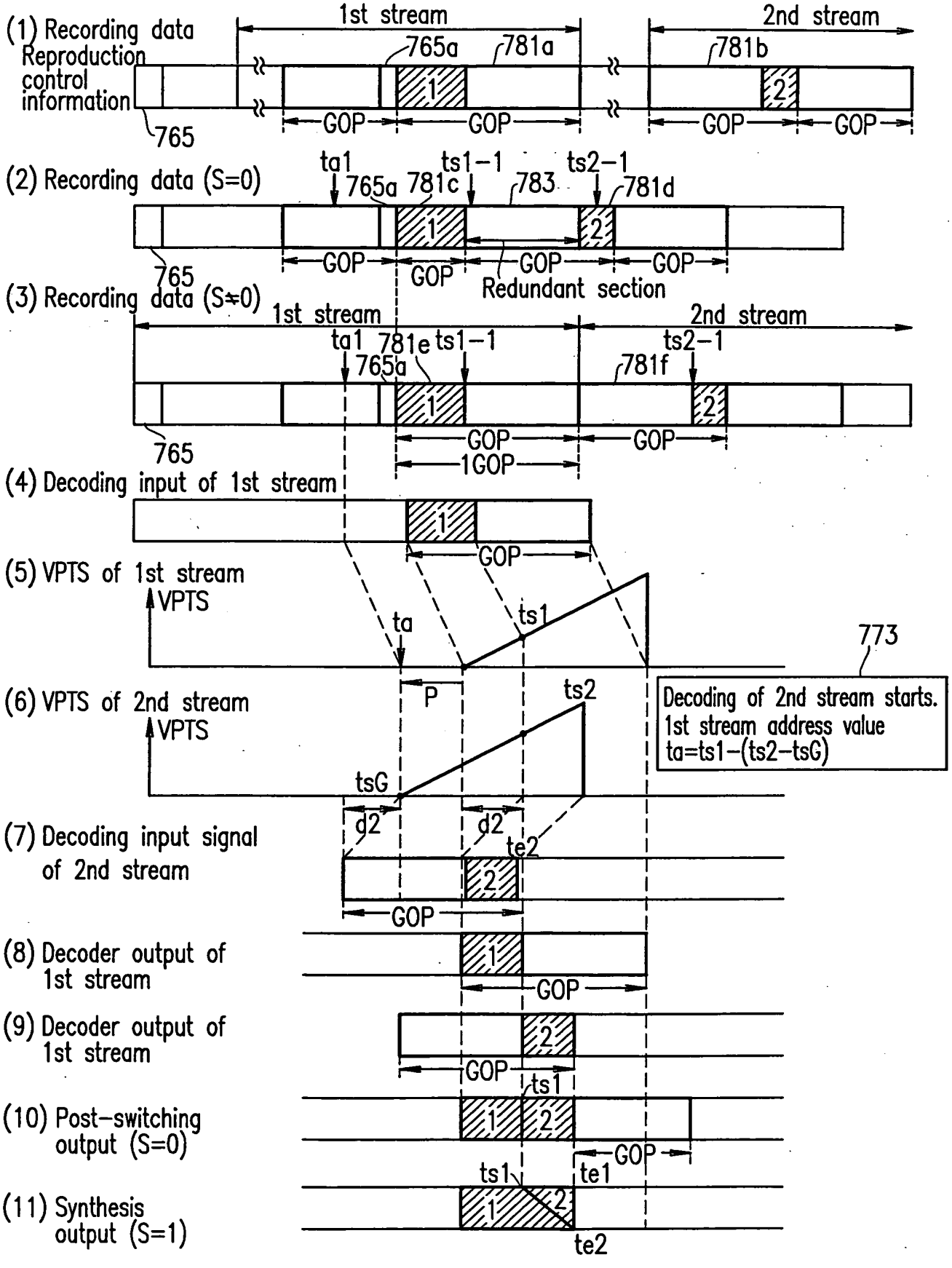

(1) Recording data Reproduction control information
1st stream
2nd stream
765a
781a
781b
765
GOP
(2) Recording data (S=0)
ta1
ts1−1
ts2−1
765a
781c
783
781d
Redundant section
(3) Recording data (S≠0)
781e
781f
1GOP
(4) Decoding input of 1st stream
(5) VPTS of 1st stream
VPTS
ta
ts1
773
(6) VPTS of 2nd stream
P
ts2
tsG
Decoding of 2nd stream starts.
1st stream address value
ta=ts1−(ts2−tsG)
(7) Decoding input signal of 2nd stream
d2
te2
(8) Decoder output of 1st stream
(9) Decoder output of 1st stream
(10) Post−switching output (S=0)
(11) Synthesis output (S=1)
te1
te2

FIG. 13

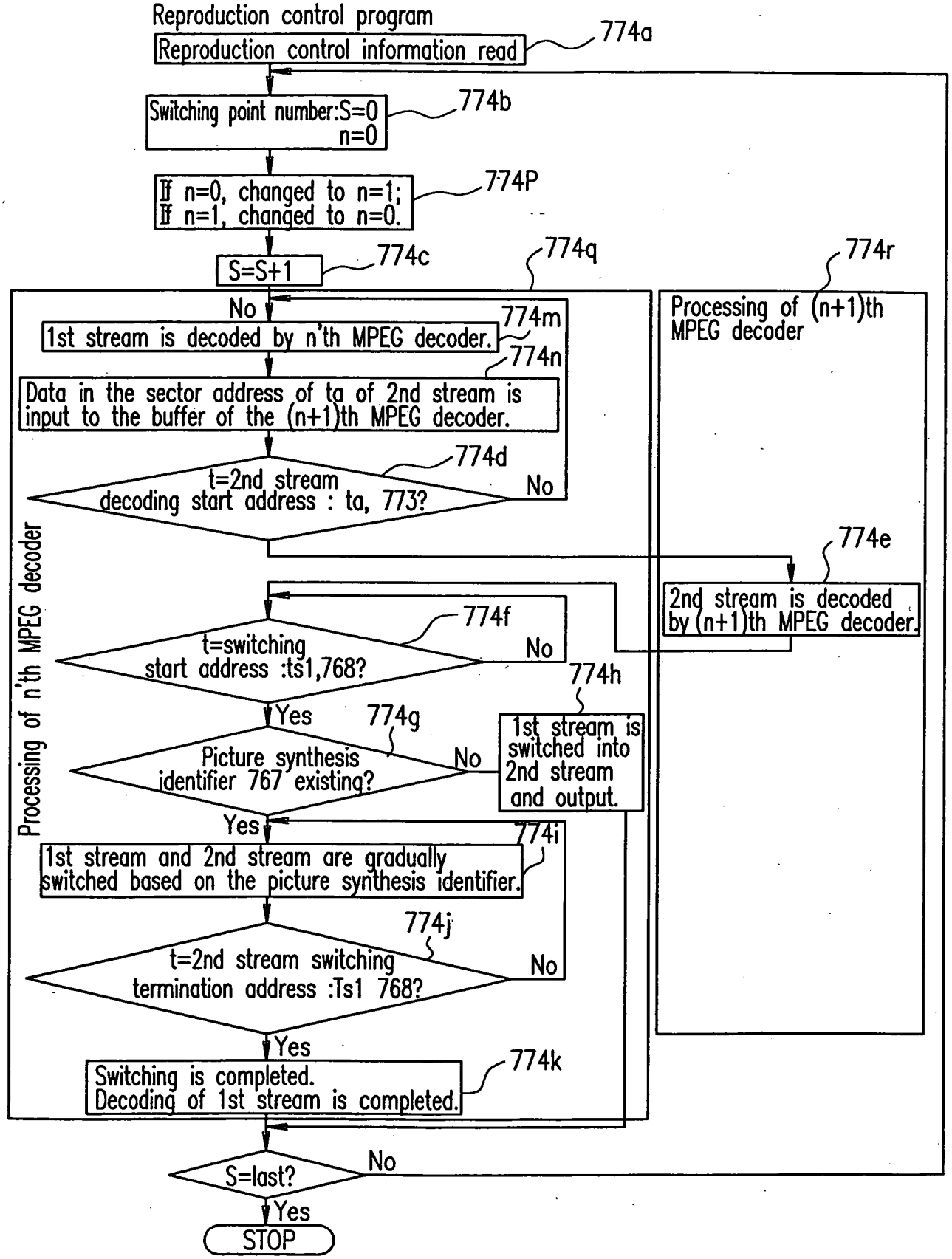

Reproduction control program
Reproduction control information read
774a
Switching point number:S=0
n=0
774b
If n=0, changed to n=1;
If n=1, changed to n=0.
774P
S=S+1
774c
774q
774r
No
1st stream is decoded by n'th MPEG decoder.
774m
Data in the sector address of ta of 2nd stream is input to the buffer of the (n+1)th MPEG decoder.
774n
t=2nd stream decoding start address : ta, 773?
774d
No
Processing of (n+1)th MPEG decoder
774e
2nd stream is decoded by (n+1)th MPEG decoder.
Processing of n'th MPEG decoder
t=switching start address :ts1,768?
774f
No
Yes
774h
1st stream is switched into 2nd stream and output.
Picture synthesis identifier 767 existing?
774g
No
Yes
1st stream and 2nd stream are gradually switched based on the picture synthesis identifier.
774i
t=2nd stream switching termination address :Ts1 768?
774j
No
Yes
Switching is completed.
Decoding of 1st stream is completed.
774k
S=last?
No
Yes
STOP

FIG. 14

Reproduction control information

766 Switching point number S	767 Picture synthesis identifier S	768 1st stream	769	770a 2nd stream	765b	771
		Switching start address : ts1	Switching termination address : te2	GOP start address : tsG Sector address:tsGs	Switching start address : ts2 Sector address	
1	None	ts1-1		tsG-1	ts2-1	
2	Mode1	ts1-2	te2-2	tsG-2	ts2-2	
3	Mode2	ts1-3	te2-3	tsG-3	ts2-3	

FIG. 15

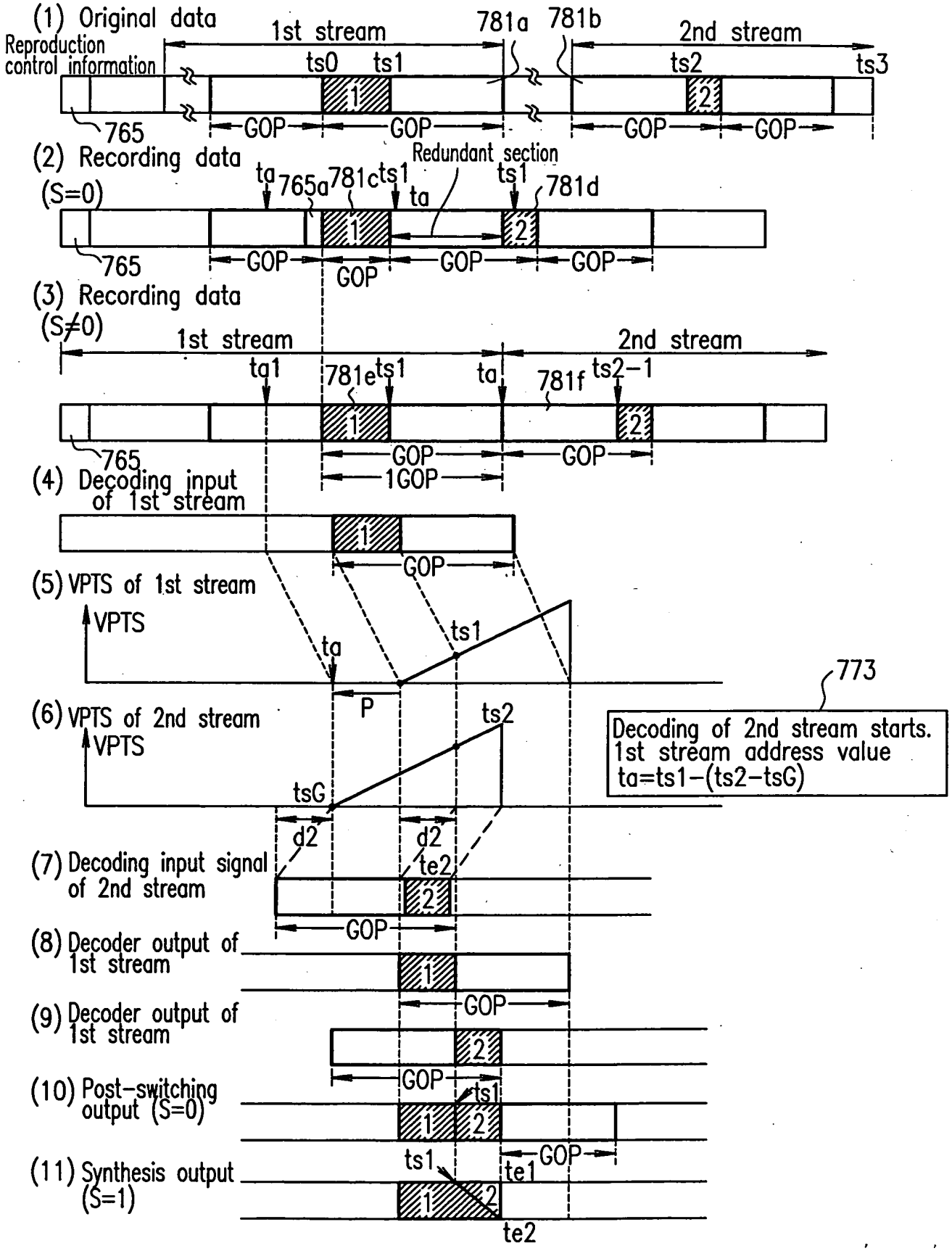

(1) Original data
Reproduction control information
1st stream
781a
781b
2nd stream
ts0
ts1
ts2
ts3
765
GOP
(2) Recording data
(S=0)
ta
765a
781c
ts1
Redundant section
781d
(3) Recording data
(S≠0)
1st stream
2nd stream
ta1
781e
781f
ts2−1
1GOP
(4) Decoding input of 1st stream
(5) VPTS of 1st stream
VPTS
P
773
Decoding of 2nd stream starts.
1st stream address value
ta=ts1−(ts2−tsG)
(6) VPTS of 2nd stream
tsG
d2
(7) Decoding input signal of 2nd stream
te2
(8) Decoder output of 1st stream
(9) Decoder output of 1st stream
(10) Post-switching output (S=0)
(11) Synthesis output (S=1)
te1

FIG. 16

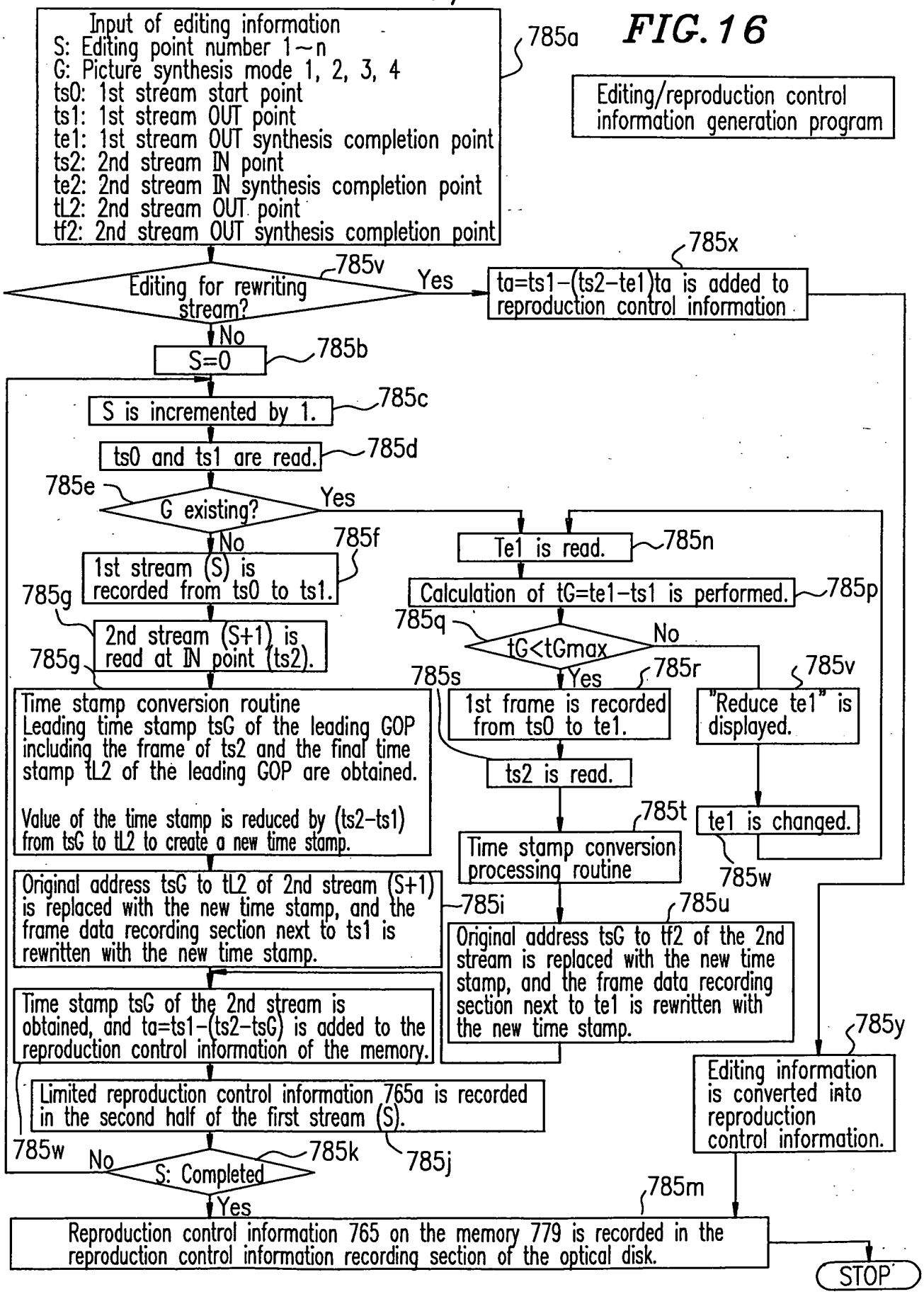

Editing/reproduction control information generation program
Input of editing information
S: Editing point number 1~n
G: Picture synthesis mode 1, 2, 3, 4
ts0: 1st stream start point
ts1: 1st stream OUT point
te1: 1st stream OUT synthesis completion point
ts2: 2nd stream IN point
te2: 2nd stream IN synthesis completion point
tL2: 2nd stream OUT point
tf2: 2nd stream OUT synthesis completion point
785a
Editing for rewriting stream?
785v
Yes
ta=ts1-(ts2-te1)ta is added to reproduction control information
785x
No
S=0
785b
S is incremented by 1.
785c
ts0 and ts1 are read.
785d
G existing?
785e
Yes
No
1st stream (S) is recorded from ts0 to ts1.
785f
2nd stream (S+1) is read at IN point (ts2).
785g
Time stamp conversion routine
Leading time stamp tsG of the leading GOP including the frame of ts2 and the final time stamp tL2 of the leading GOP are obtained.
Value of the time stamp is reduced by (ts2-ts1) from tsG to tL2 to create a new time stamp.
Original address tsG to tL2 of 2nd stream (S+1) is replaced with the new time stamp, and the frame data recording section next to ts1 is rewritten with the new time stamp.
785i
Time stamp tsG of the 2nd stream is obtained, and ta=ts1-(ts2-tsG) is added to the reproduction control information of the memory.
Limited reproduction control information 765a is recorded in the second half of the first stream (S).
785j
S: Completed
785k
No
Yes
785w
Te1 is read.
785n
Calculation of tG=te1-ts1 is performed.
785p
tG<tGmax
785q
No
Yes
1st frame is recorded from ts0 to te1.
785r
"Reduce te1" is displayed.
785v
ts2 is read.
785s
te1 is changed.
785w
Time stamp conversion processing routine
785t
Original address tsG to tf2 of the 2nd stream is replaced with the new time stamp, and the frame data recording section next to te1 is rewritten with the new time stamp.
785u
Editing information is converted into reproduction control information.
785y
Reproduction control information 765 on the memory 779 is recorded in the reproduction control information recording section of the optical disk.
785m
STOP

FIG. 17 Progressive/3D image arrangement information (resolution/picture identification information)

83 ~ TXTDT file | PGC file in each VTS ~ 744

14

VTS (title)	Cell	TXTDT information: Attribute	TXTDT information: Number of multiple angles	Angle		Start address	Termination address	Identification information
1	1, 2	3D Cell1, 2	2	1	Main	a_1	a_3	3D–right
				2	Sub	a_2	a_4	3D–left
2	1, 2	3D Cell1, 2	2	1	Main	a_5	a_7	3D–right
				2	Sub	a_6	a_8	3D–left
	3, 4	Progressive 480P X multiple angles (Cell1, 2)	4	1	Main	a_9	a_{11}	1–480P–main
				2	Sub	a_{10}	a_{12}	1–480P–sub
				3	Main	a_{13}	a_{15}	2–480P–main
				4	Sub	a_{14}	a_{16}	2–480P–sub
3	1, 2	Wide480P (Cell1, 2)	2	1	Main	a_{17}	a_{19}	Wide480i–main
				2	Sub	a_{18}	a_{20}	Wide480i–sub
4	1, 2	Wide480P	4	1	Main	a_{21}	a_{22}	Wide480P–main main
				2	Sub	a_{23}	a_{24}	Wide480P–main sub
				3	Main	a_{25}	a_{26}	Wide480P–sub main
				4	Sub	a_{27}	a_{28}	Wide480P–sub sub
5	1, 2 3, 4	3D480P	4	1	Main	a_{29}	a_{30}	Right480P–main
				2	Sub	a_{31}	a_{32}	Right480P–sub
				3	Main	a_{33}	a_{34}	Left480P–main
				4	Sub	a_{35}	a_{36}	Left480P–sub
6	1, 2	720P (24fps)	2	1	Main	a_{37}	a_{38}	720P–main
				2	Sub	a_{39}	a_{40}	720P–sub

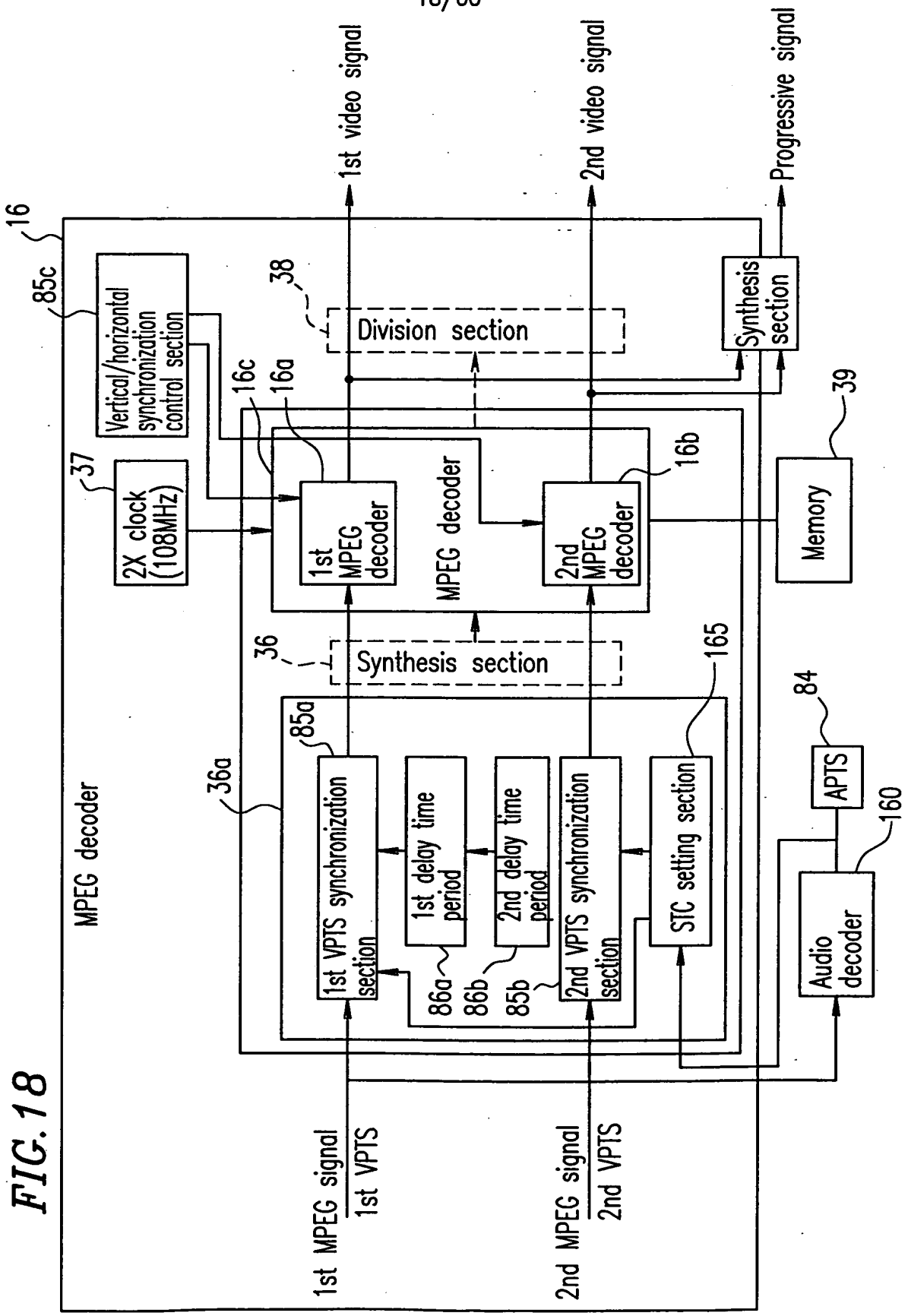
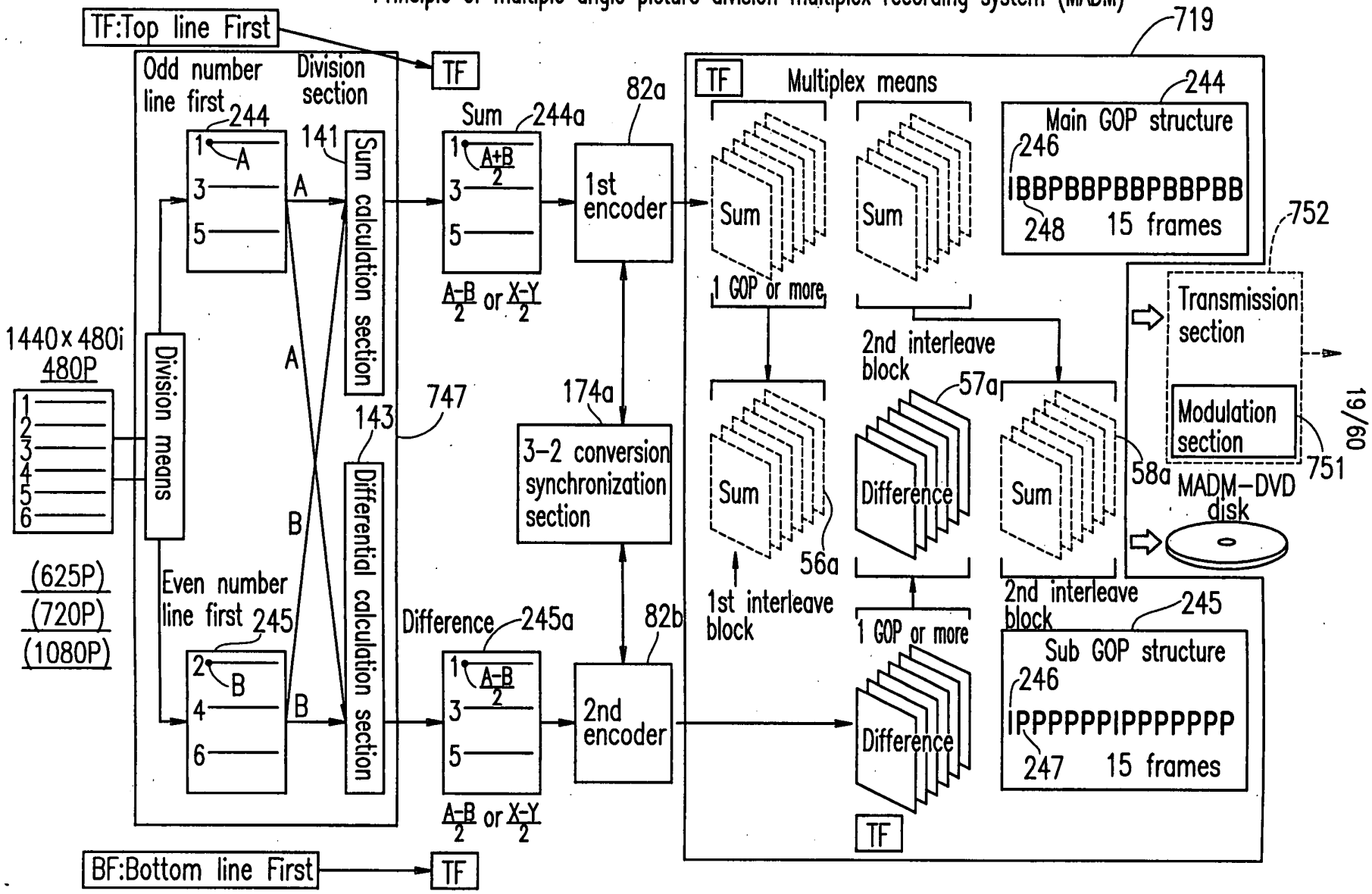

MPEG decoder
16
1st video signal
2nd video signal
Progressive signal
85c
Vertical/horizontal synchronization control section
38
Division section
Synthesis section
16c
16a
16b
39
37
2X clock (108MHz)
1st MPEG decoder
MPEG decoder
2nd MPEG decoder
Memory
36
Synthesis section
165
84
85a
36a
1st VPTS synchronization section
1st delay time period
2nd delay time period
2nd VPTS synchronization section
STC setting section
APTS
160
86a
86b
85b
Audio decoder
1st MPEG signal
1st VPTS
2nd MPEG signal
2nd VPTS

FIG. 18

FIG. 19

Principle of multiple angle picture division multiplex recording system (MADM)



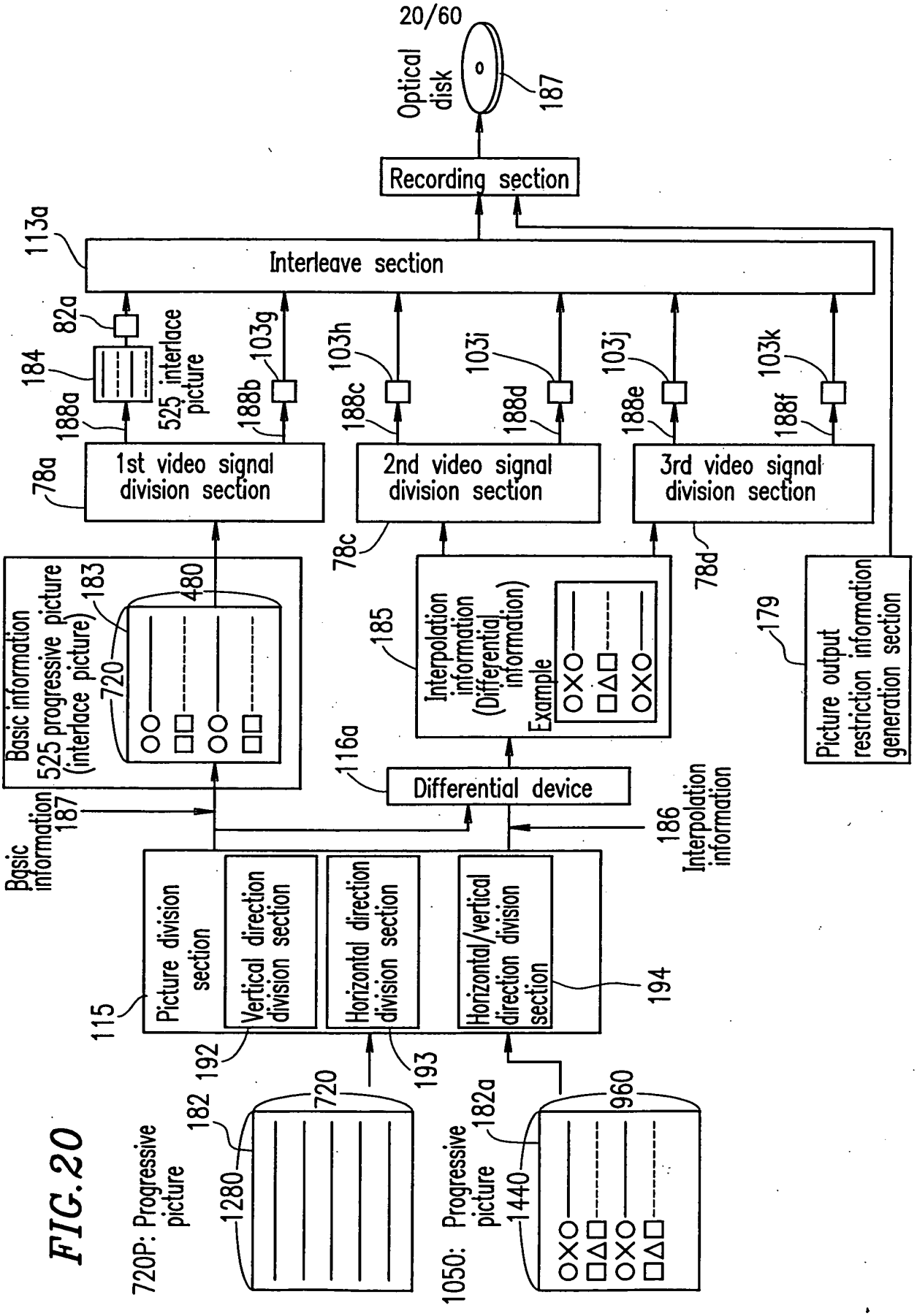

20/60
Optical disk
187
Recording section
113a
Interleave section
82a
184
525 interlace picture
188a
188b
103g
103h
188c
103i
188d
103j
188e
103k
188f
78a
1st video signal division section
2nd video signal division section
3rd video signal division section
78c
78d
Basic information 525 progressive picture (interlace picture)
183
480
720
185
Interpolation information (Differential information)
Example
179
Picture output restriction information generation section
116a
Differential device
Basic information 187
186 Interpolation information
115
Picture division section
Vertical direction division section
Horizontal direction division section
Horizontal/vertical direction division section
194
192
193
182
720
1280
720P: Progressive picture
182a
960
1440
1050: Progressive picture

FIG. 20

FIG.21

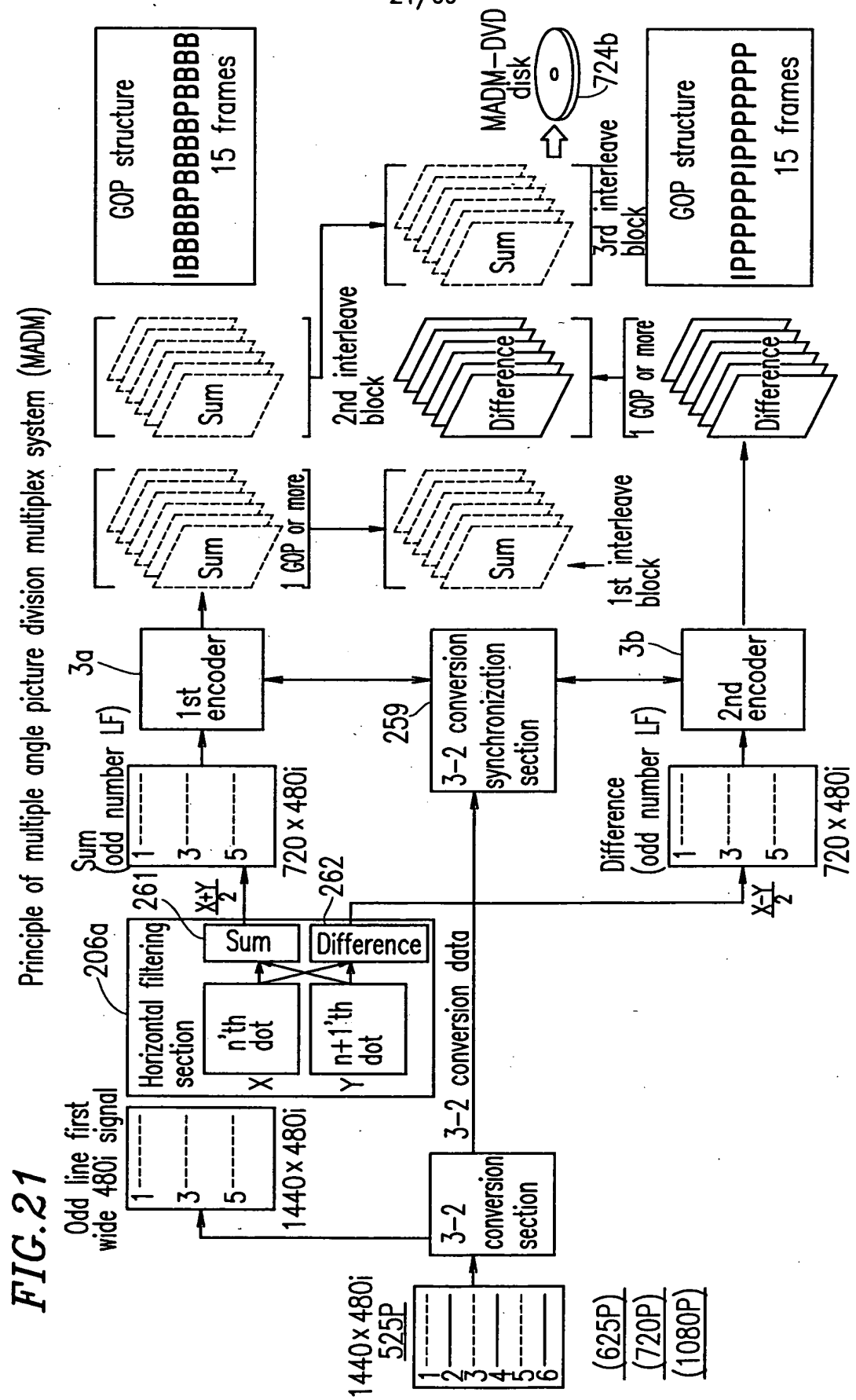

Principle of multiple angle picture division multiplex system (MADM)
1440 x 480i
525P
(625P)
(720P)
(1080P)
3-2 conversion section
Odd line first wide 480i signal
1440 x 480i
3-2 conversion data
206a
Horizontal filtering section
n'th dot
n+1'th dot
X
Y
Sum
Difference
261
262
X+Y/2
Sum (odd number LF)
720 x 480i
259
3-2 conversion synchronization section
Difference (odd number LF)
720 x 480i
3a
1st encoder
3b
2nd encoder
1 GOP or more
1st interleave block
2nd interleave block
3rd interleave block
GOP structure
IBBBBPBBBBPBBBB
15 frames
GOP structure
IPPPPPIPPPPPPP
15 frames
MADM-DVD disk
724b

FIG.22

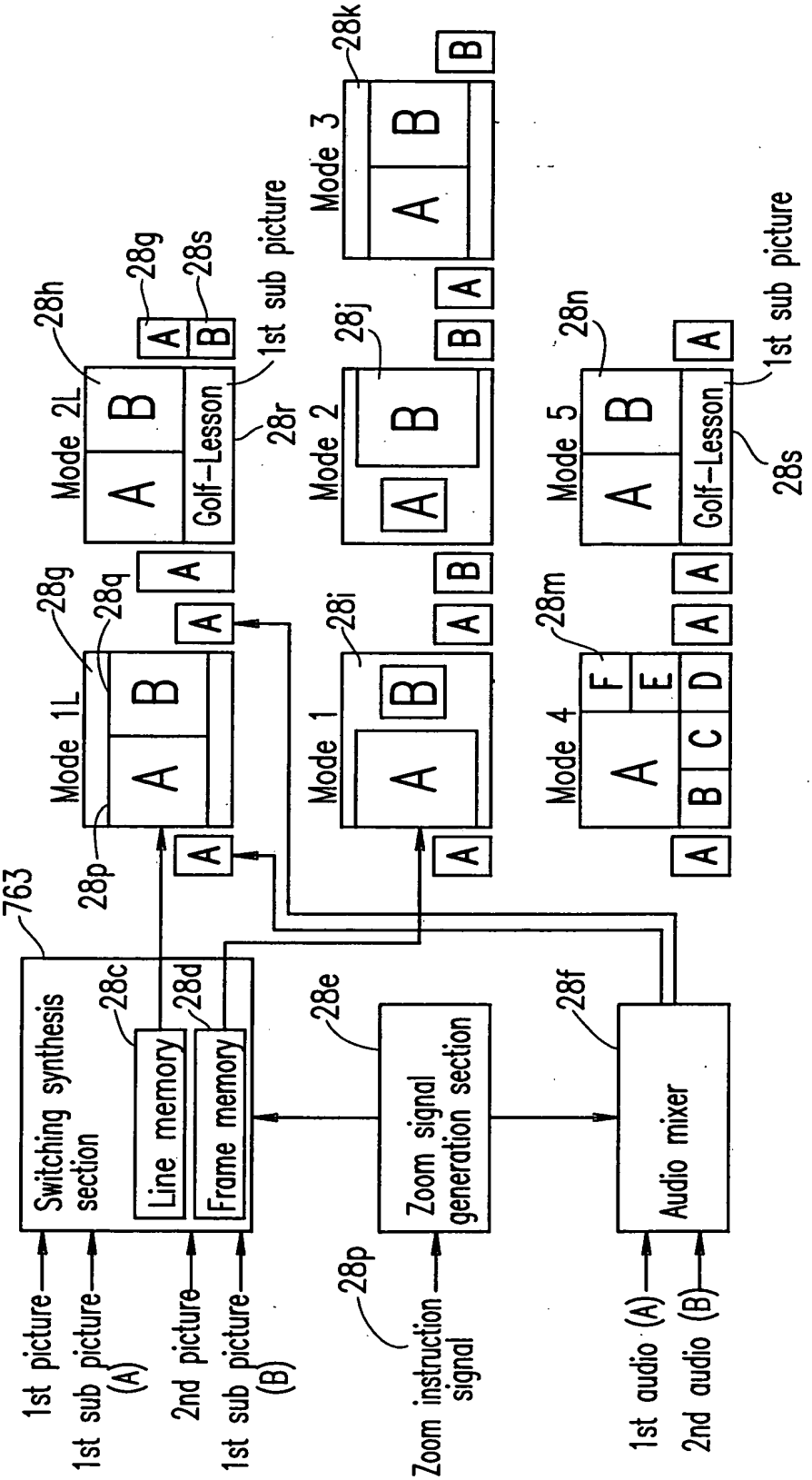
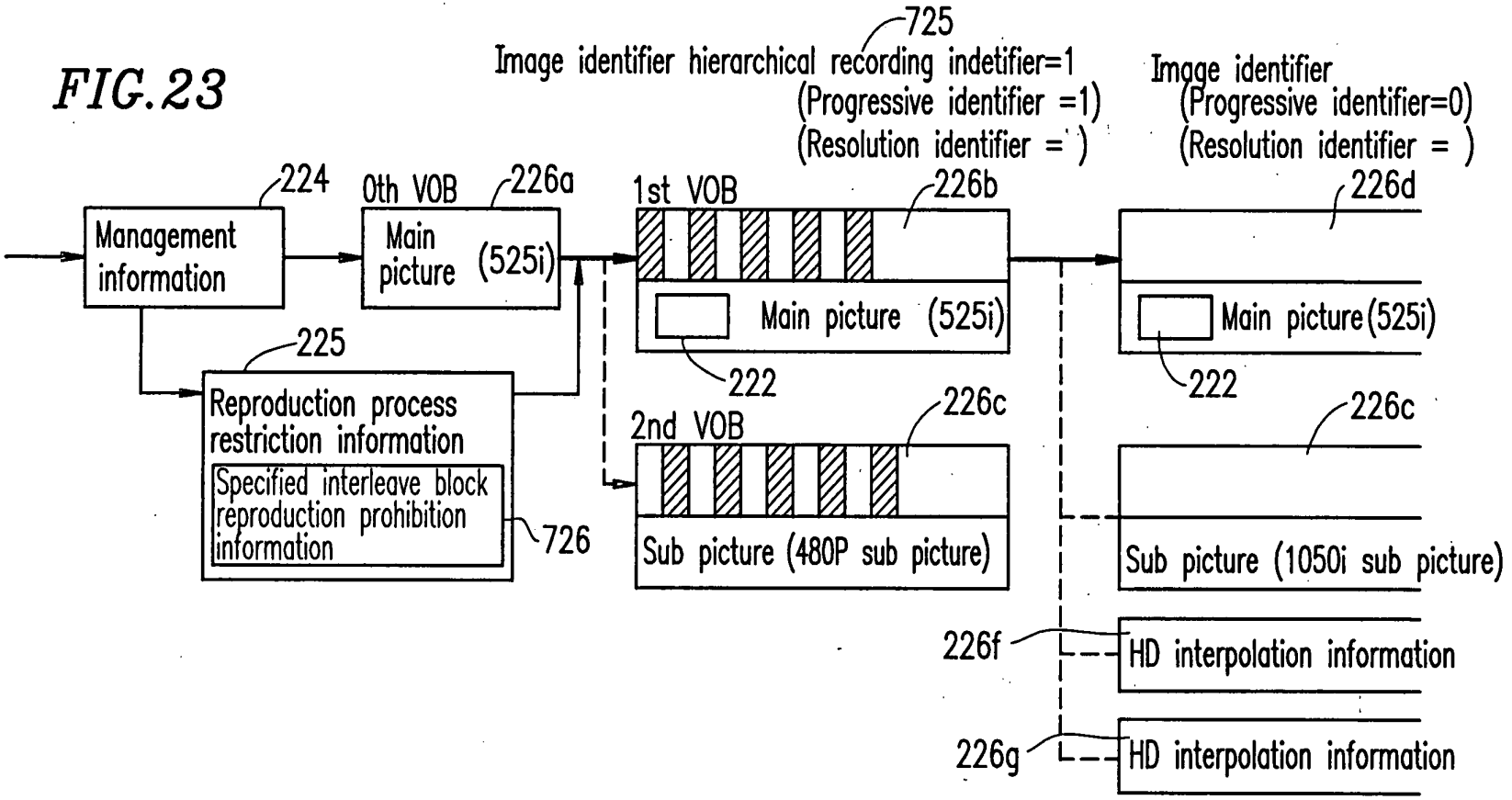
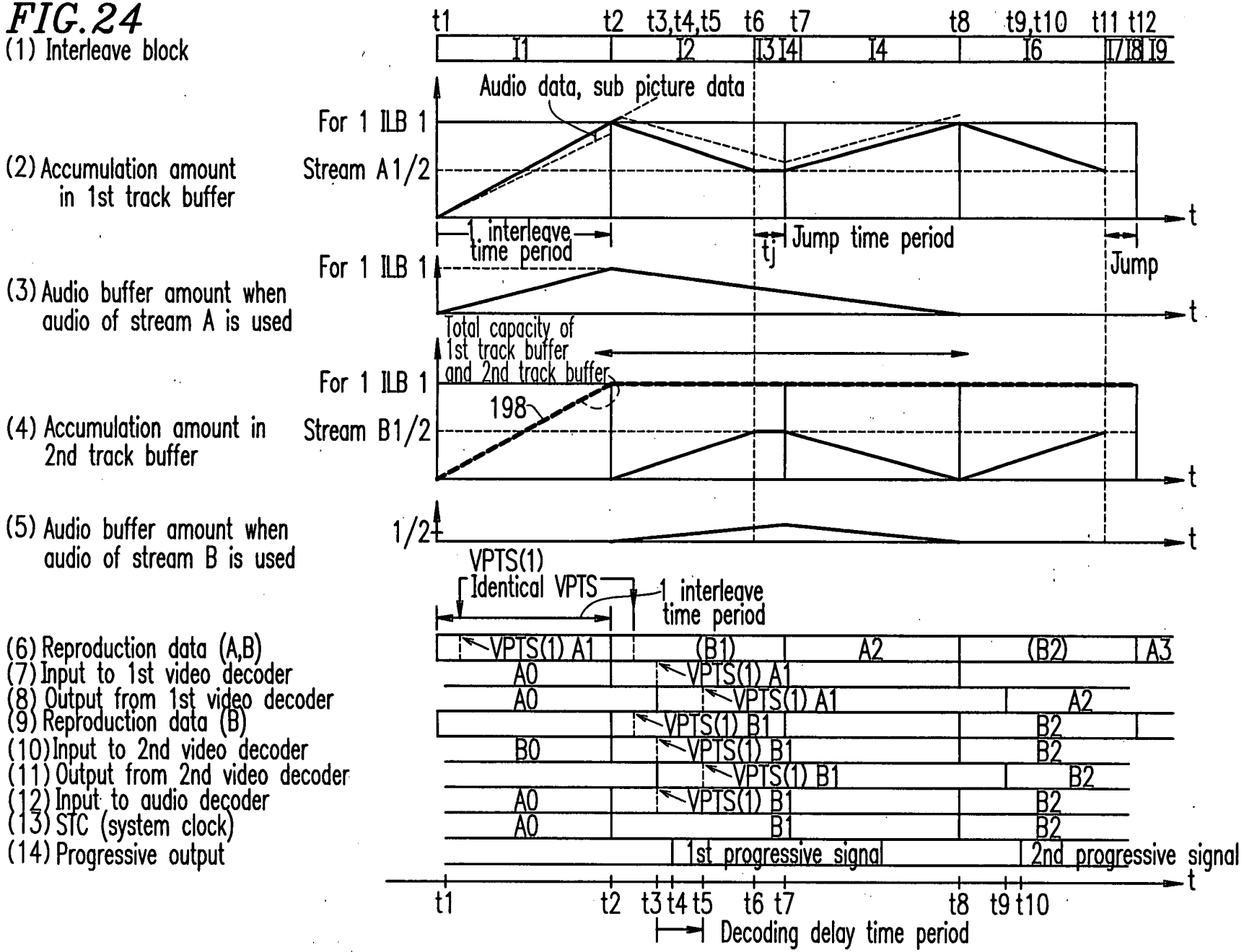

763
Switching synthesis section
28c
Line memory
28d
Frame memory
28e
Zoom signal generation section
28f
Audio mixer
1st picture
1st sub picture (A)
2nd picture
1st sub picture (B)
28p
Zoom instruction signal
1st audio (A)
2nd audio (B)
Mode 1L
28g
28q
28p
Mode 2L
28h
28g
28s
28r
Golf-Lesson
1st sub picture
Mode 1
28i
Mode 2
28j
Mode 3
28k
Mode 4
28m
Mode 5
28n
28s
Golf-Lesson
1st sub picture

FIG.23



Conventional player	NTSC(525i)	NTSC(525i)	NTSC(525i)
Progressive player	NTSC(525i)	Progressive(525i)	1050i
HD player	NTSC	(525P)	HDTV(720P)

FIG.24


(1) Interleave block
t1
t2
t3,t4,t5
t6
t7
t8
t9,t10
t11 t12
I1
I2
I3 I4
I4
I6
I7 I8 I9
(2) Accumulation amount in 1st track buffer
Audio data, sub picture data
For 1 ILB 1
Stream A1/2
1 interleave time period
Jump time period
tj
Jump
t
(3) Audio buffer amount when audio of stream A is used
For 1 ILB 1
Total capacity of 1st track buffer and 2nd track buffer
(4) Accumulation amount in 2nd track buffer
For 1 ILB 1
198
Stream B1/2
(5) Audio buffer amount when audio of stream B is used
1/2
VPTS(1)
Identical VPTS
1 interleave time period
(6) Reproduction data (A,B)
(7) Input to 1st video decoder
(8) Output from 1st video decoder
(9) Reproduction data (B)
(10) Input to 2nd video decoder
(11) Output from 2nd video decoder
(12) Input to audio decoder
(13) STC (system clock)
(14) Progressive output
VPTS(1) A1
(B1)
A2
(B2)
A3
A0
B0
B1
B2
1st progressive signal
2nd progressive signal
Decoding delay time period

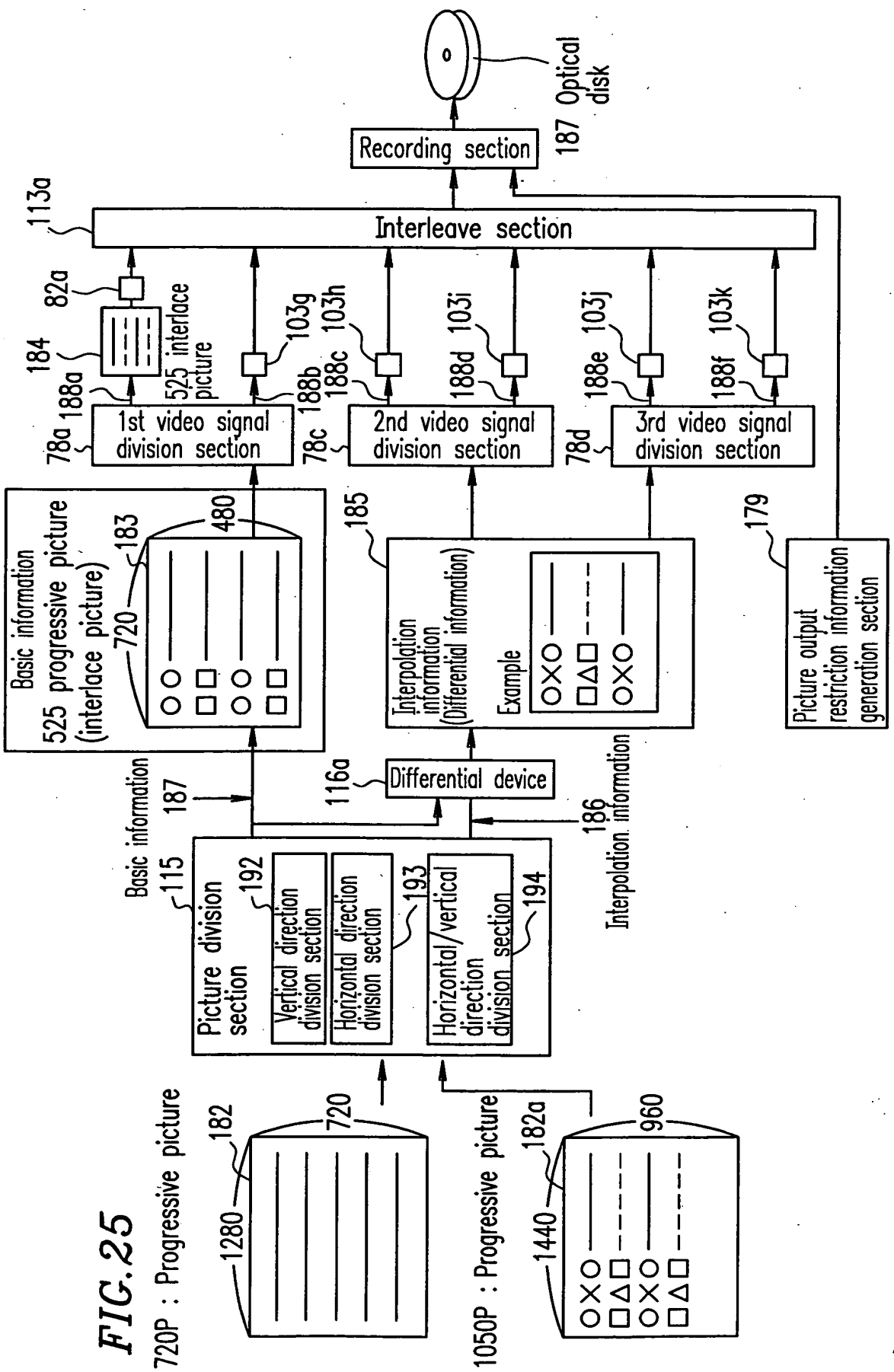

Optical disk
187
Recording section
Interleave section
113a
82a
184
525 interlace picture
188a
103g
103h
103i
103j
103k
188b
188c
188d
188e
188f
1st video signal division section
2nd video signal division section
3rd video signal division section
78a
78c
78d
Basic information
525 progressive picture (interlace picture)
183
480
720
185
Interpolation information (Differential information)
Example
179
Picture output restriction information generation section
Basic information
187
116a
Differential device
186
Interpolation information
115
Picture division section
192
Vertical direction division section
Horizontal direction division section
193
Horizontal/vertical direction division section
194
720P : Progressive picture
182
1280
720
1050P : Progressive picture
182a
1440
960

FIG.25

FIG. 26

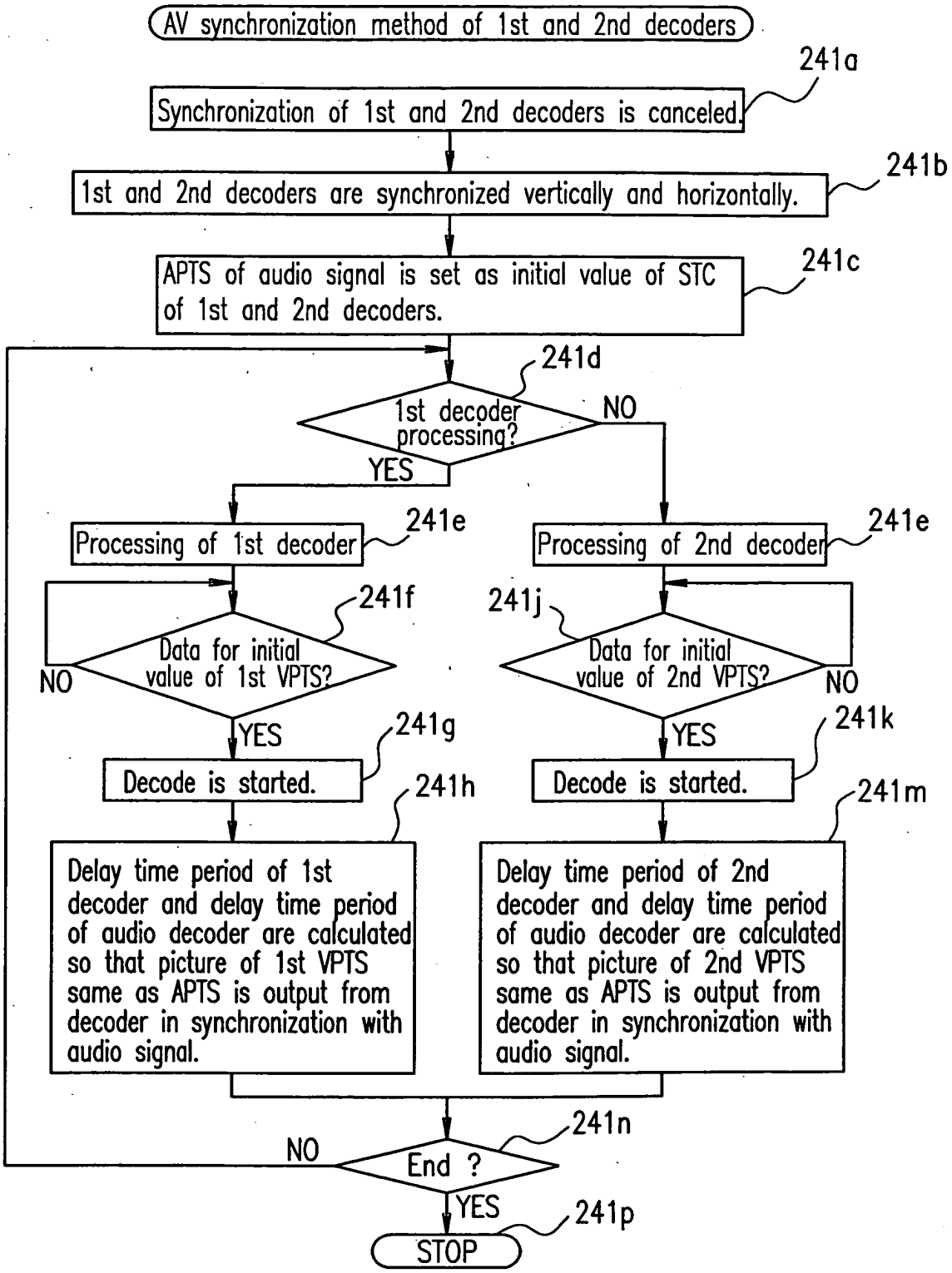

AV synchronization method of 1st and 2nd decoders
241a
Synchronization of 1st and 2nd decoders is canceled.
241b
1st and 2nd decoders are synchronized vertically and horizontally.
241c
APTS of audio signal is set as initial value of STC of 1st and 2nd decoders.
241d
1st decoder processing?
NO
YES
Processing of 1st decoder
241e
Processing of 2nd decoder
241e
241f
Data for initial value of 1st VPTS?
NO
YES
241j
Data for initial value of 2nd VPTS?
NO
YES
241g
Decode is started.
241k
Decode is started.
241h
Delay time period of 1st decoder and delay time period of audio decoder are calculated so that picture of 1st VPTS same as APTS is output from decoder in synchronization with audio signal.
241m
Delay time period of 2nd decoder and delay time period of audio decoder are calculated so that picture of 2nd VPTS same as APTS is output from decoder in synchronization with audio signal.
241n
End ?
NO
YES
241p
STOP

FIG.27

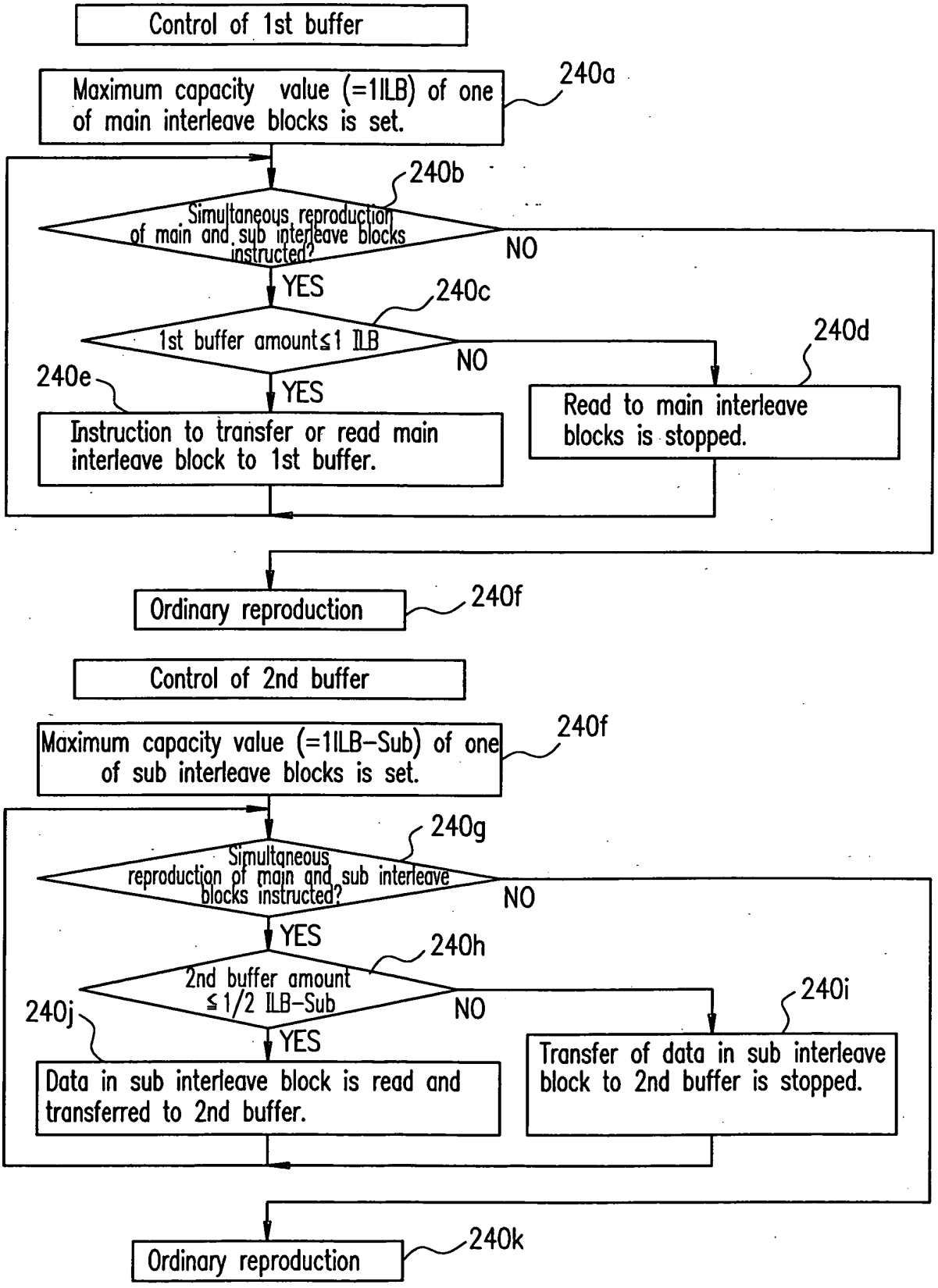

Control of 1st buffer
Maximum capacity value (=1ILB) of one of main interleave blocks is set.
240a
240b
Simultaneous reproduction of main and sub interleave blocks instructed?
NO
YES
240c
1st buffer amount≤1 ILB
NO
240d
YES
240e
Instruction to transfer or read main interleave block to 1st buffer.
Read to main interleave blocks is stopped.
Ordinary reproduction
240f
Control of 2nd buffer
Maximum capacity value (=1ILB-Sub) of one of sub interleave blocks is set.
240f
240g
Simultaneous reproduction of main and sub interleave blocks instructed?
NO
YES
240h
2nd buffer amount ≤1/2 ILB-Sub
NO
240i
240j
YES
Data in sub interleave block is read and transferred to 2nd buffer.
Transfer of data in sub interleave block to 2nd buffer is stopped.
Ordinary reproduction
240k

FIG. 28

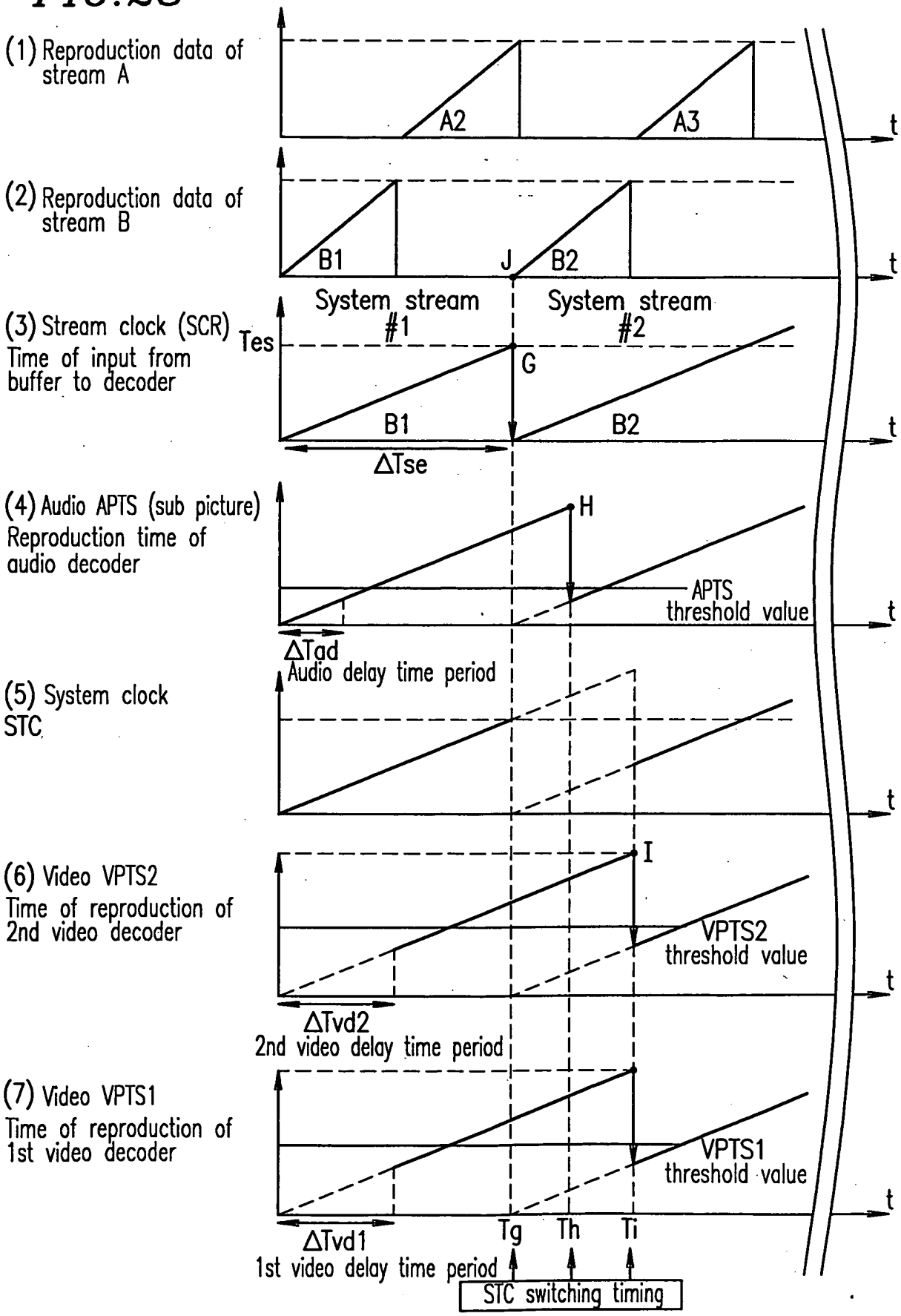
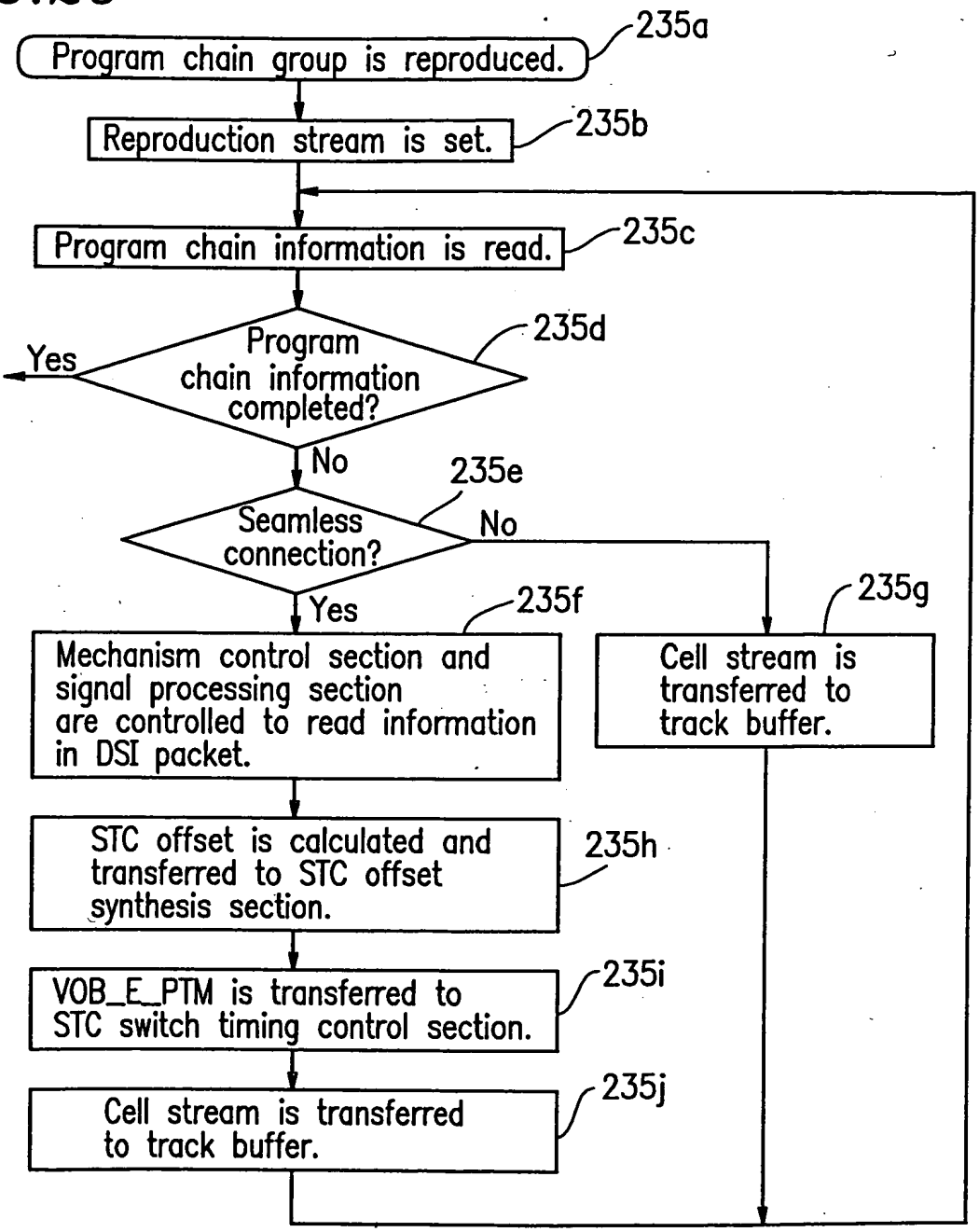

(1) Reproduction data of stream A
A2
A3
t
(2) Reproduction data of stream B
B1
J
B2
t
(3) Stream clock (SCR)
Time of input from buffer to decoder
System stream #1
System stream #2
Tes
G
B1
B2
t
ΔTse
(4) Audio APTS (sub picture)
Reproduction time of audio decoder
H
APTS threshold value
t
ΔTad
Audio delay time period
(5) System clock STC
t
(6) Video VPTS2
Time of reproduction of 2nd video decoder
I
VPTS2 threshold value
t
ΔTvd2
2nd video delay time period
(7) Video VPTS1
Time of reproduction of 1st video decoder
VPTS1 threshold value
t
ΔTvd1
1st video delay time period
Tg
Th
Ti
STC switching timing

FIG.29


Program chain group is reproduced.
235a
Reproduction stream is set.
235b
Program chain information is read.
235c
Program chain information completed?
235d
Yes
No
Seamless connection?
235e
No
Yes
Mechanism control section and signal processing section are controlled to read information in DSI packet.
235f
Cell stream is transferred to track buffer.
235g
STC offset is calculated and transferred to STC offset synthesis section.
235h
VOB_E_PTM is transferred to STC switch timing control section.
235i
Cell stream is transferred to track buffer.
235j

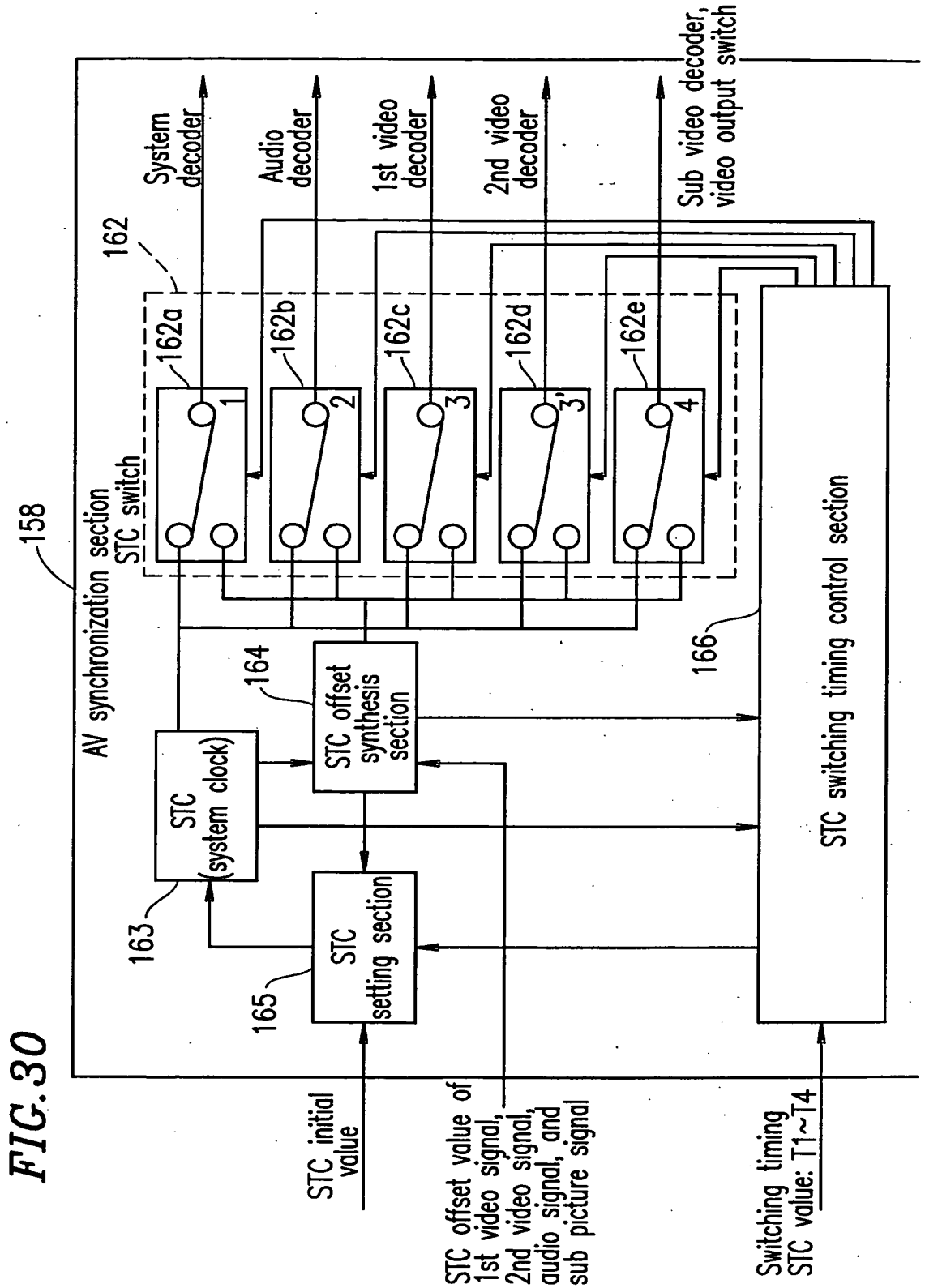

158
AV synchronization section
STC switch
162
162a
162b
162c
162d
162e
1
2
3
3'
4
System decoder
Audio decoder
1st video decoder
2nd video decoder
Sub video decoder, video output switch
164
STC offset synthesis section
166
STC switching timing control section
STC (system clock)
163
STC setting section
165
STC initial value
STC offset value of 1st video signal, 2nd video signal, audio signal, and sub picture signal
Switching timing STC value: T1~T4

FIG. 30

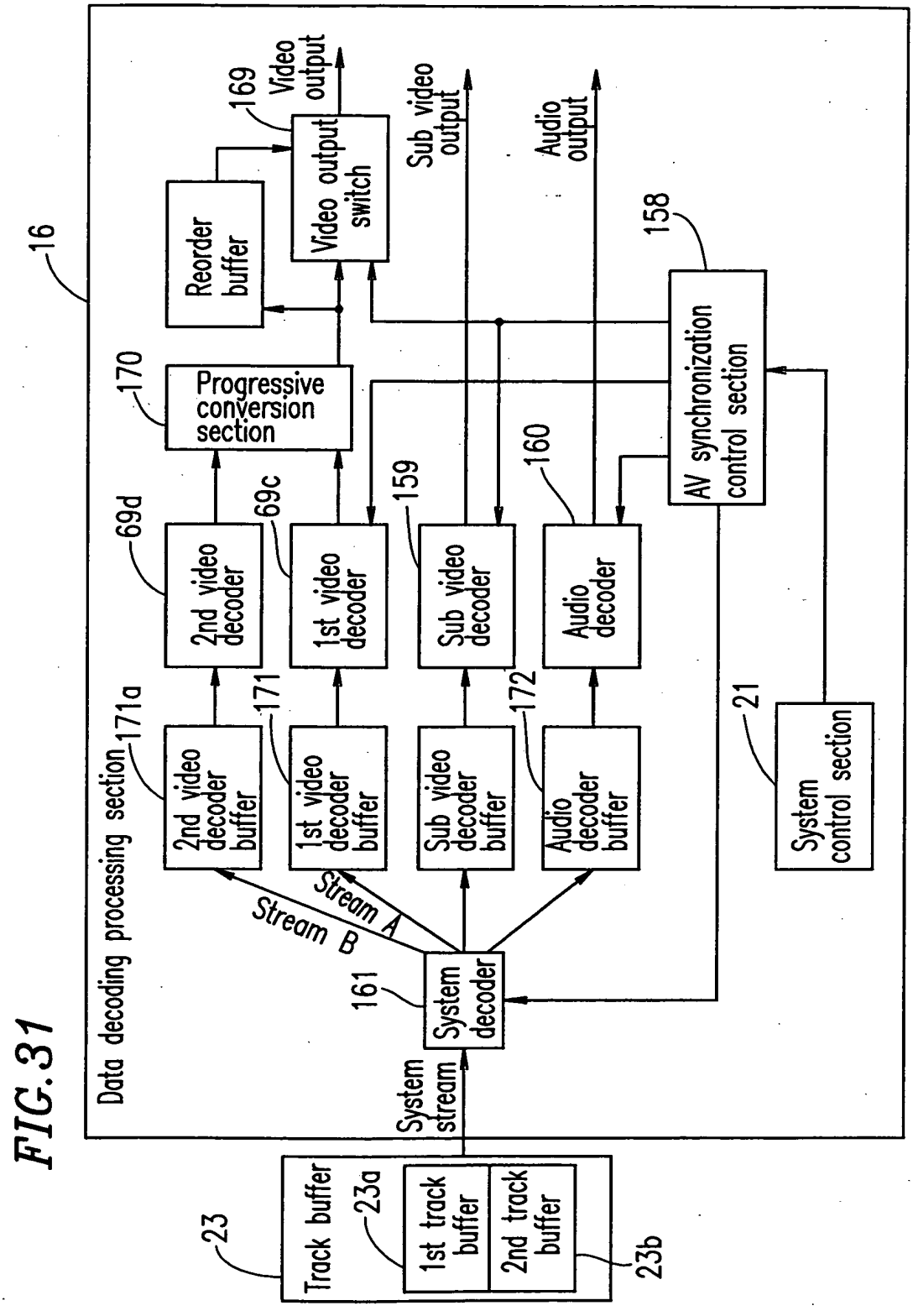


FIG. 31

FIG. 32

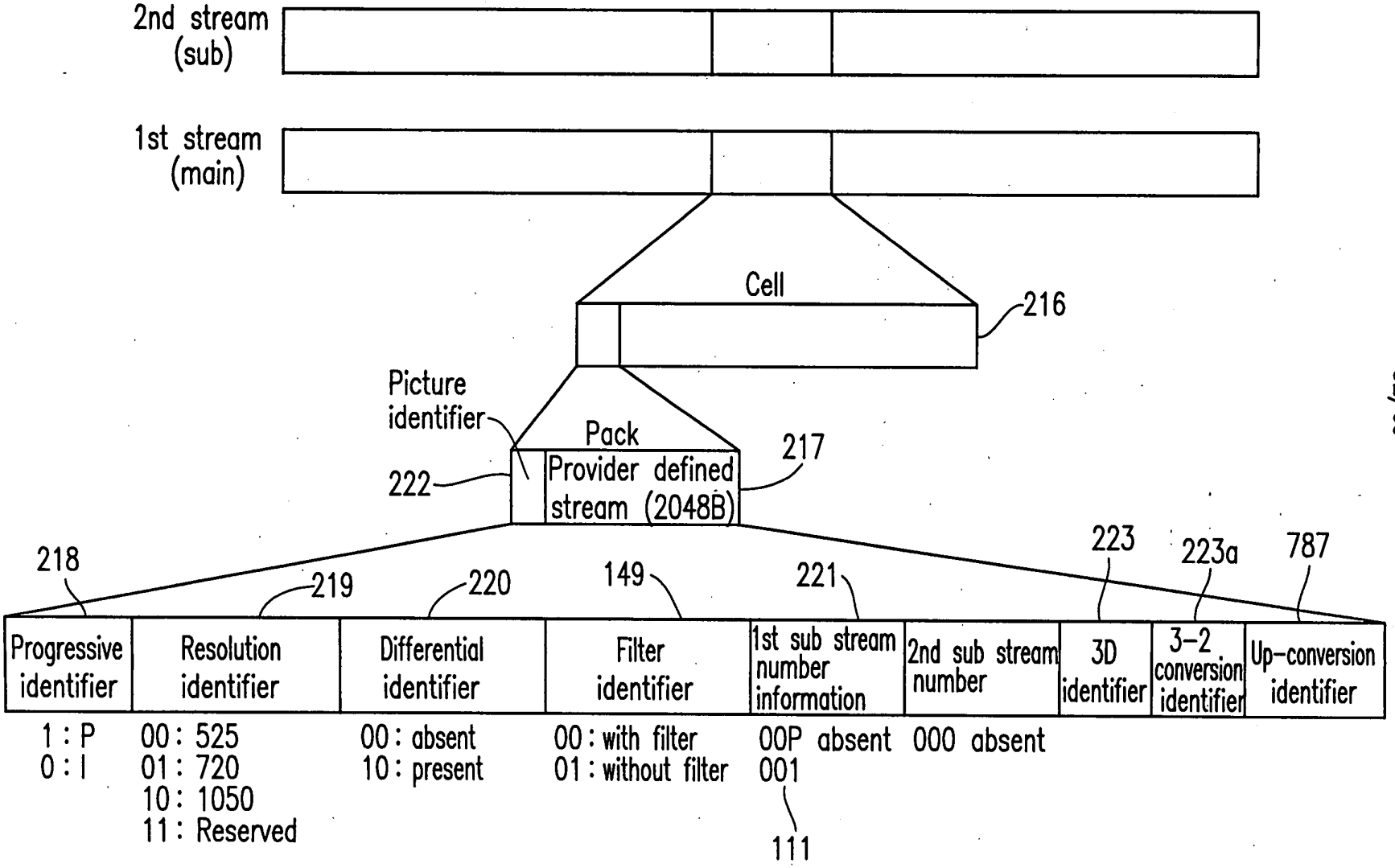


FIG. 33

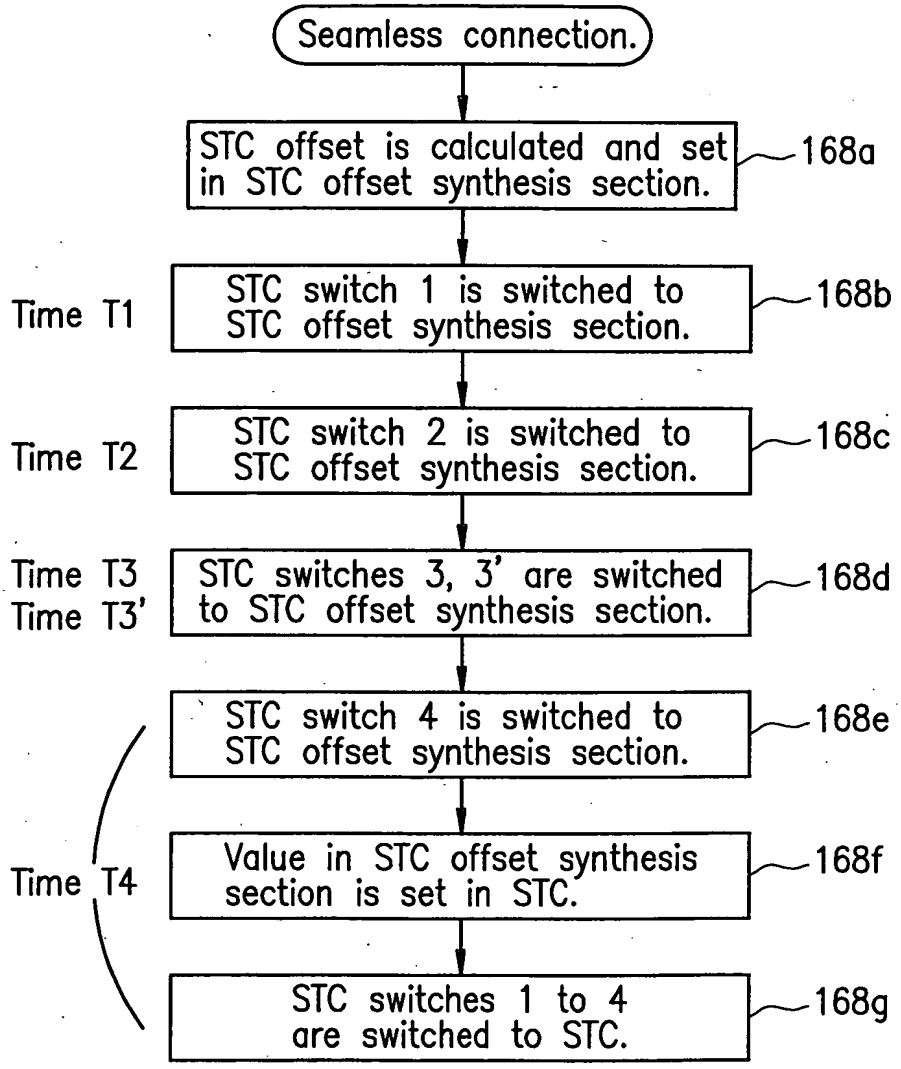
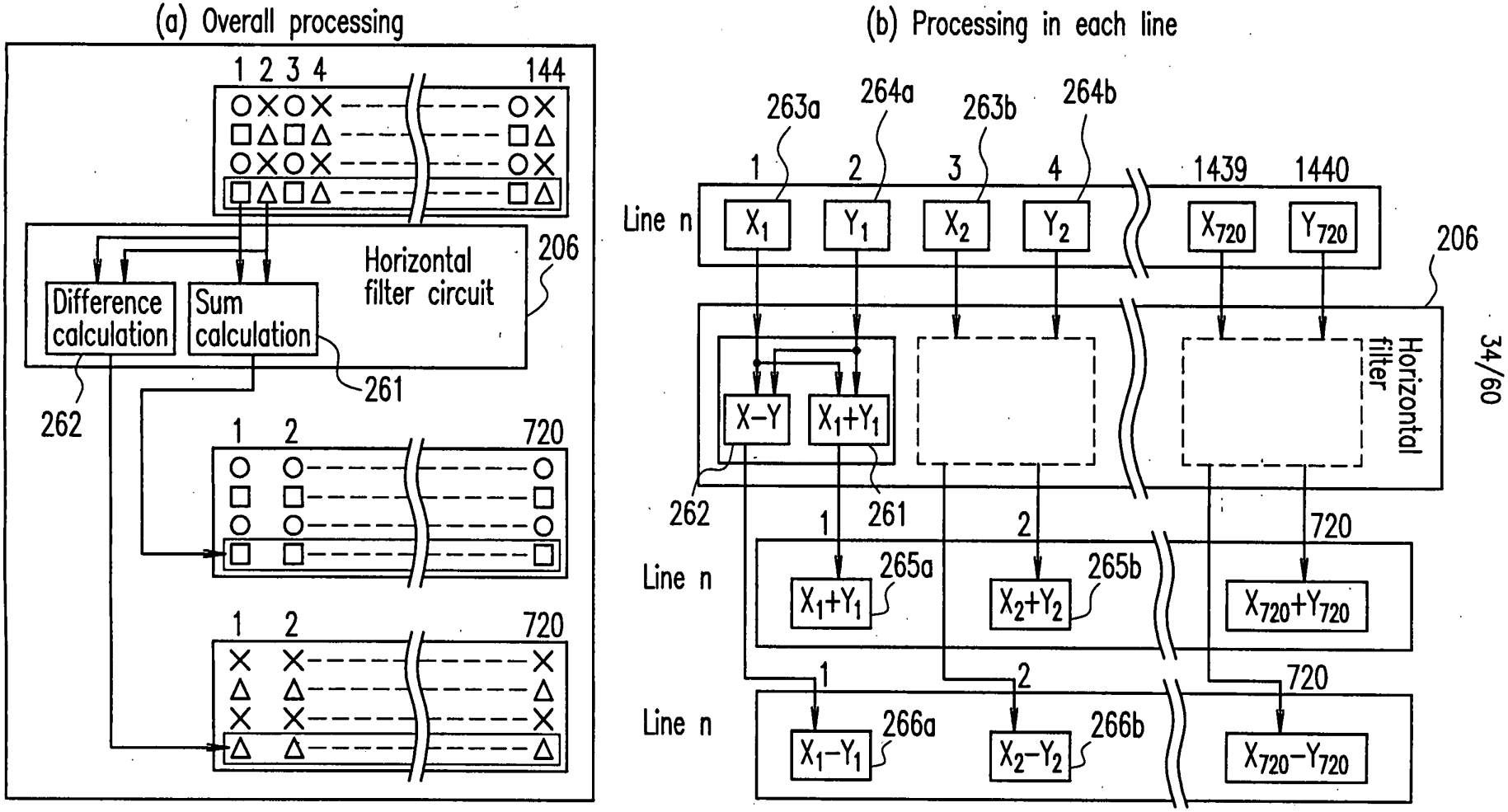

Seamless connection.
STC offset is calculated and set in STC offset synthesis section.
168a
Time T1
STC switch 1 is switched to STC offset synthesis section.
168b
Time T2
STC switch 2 is switched to STC offset synthesis section.
168c
Time T3
Time T3'
STC switches 3, 3' are switched to STC offset synthesis section.
168d
STC switch 4 is switched to STC offset synthesis section.
168e
Time T4
Value in STC offset synthesis section is set in STC.
168f
STC switches 1 to 4 are switched to STC.
168g

FIG. 34


(a) Overall processing
1 2 3 4
144
Horizontal filter circuit
206
Difference calculation
Sum calculation
261
262
1 2
720
1 2
720
(b) Processing in each line
263a
264a
263b
264b
1
2
3
4
1439
1440
Line n
X1
Y1
X2
Y2
X720
Y720
206
Horizontal filter
X-Y
X1+Y1
262
1
261
2
720
Line n
265a
265b
X1+Y1
X2+Y2
X720+Y720
1
2
720
Line n
266a
266b
X1-Y1
X2-Y2
X720-Y720

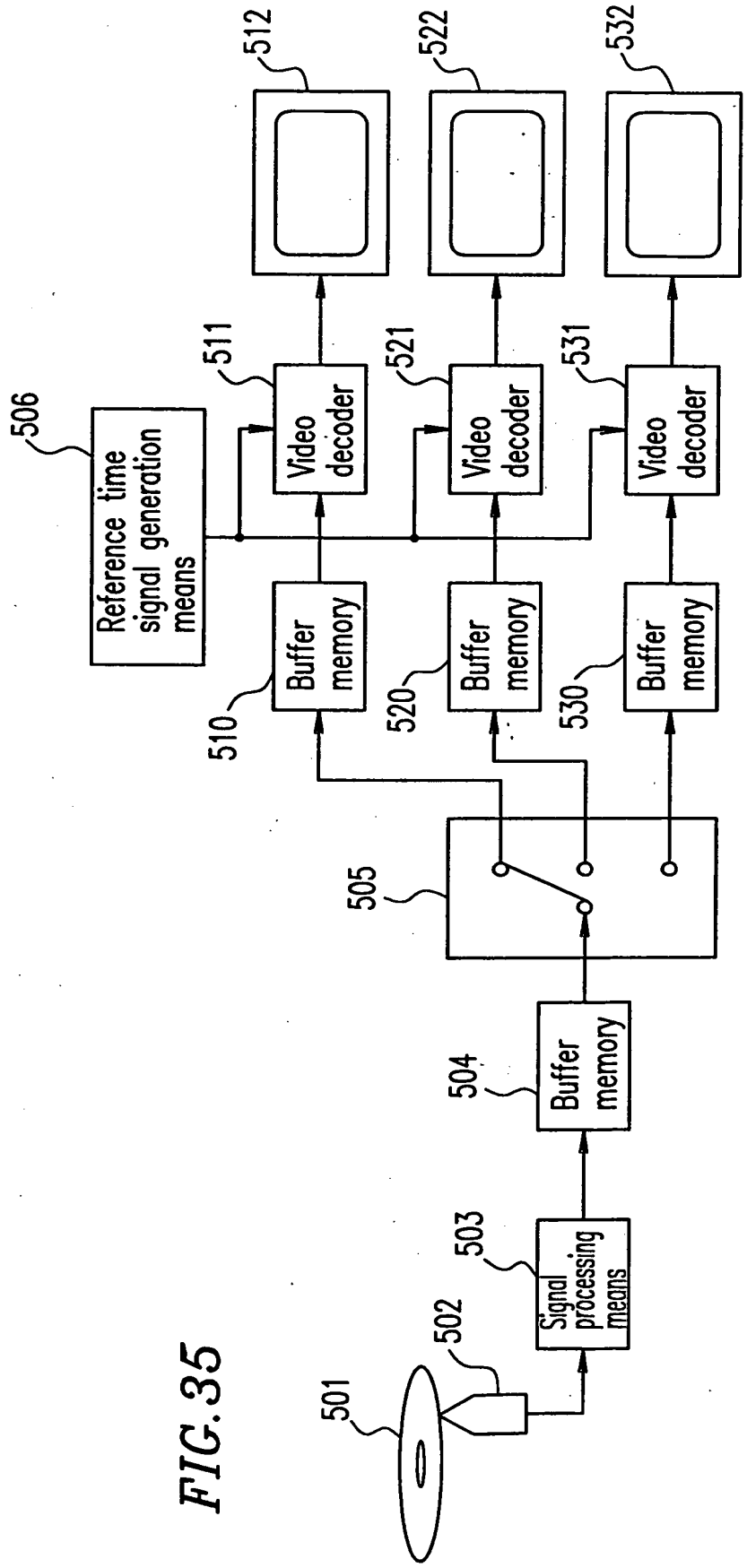

501
502
503
Signal processing means
504
Buffer memory
505
510
Buffer memory
520
Buffer memory
530
Buffer memory
506
Reference time signal generation means
511
Video decoder
521
Video decoder
531
Video decoder
512
522
532

FIG.35

FIG.36

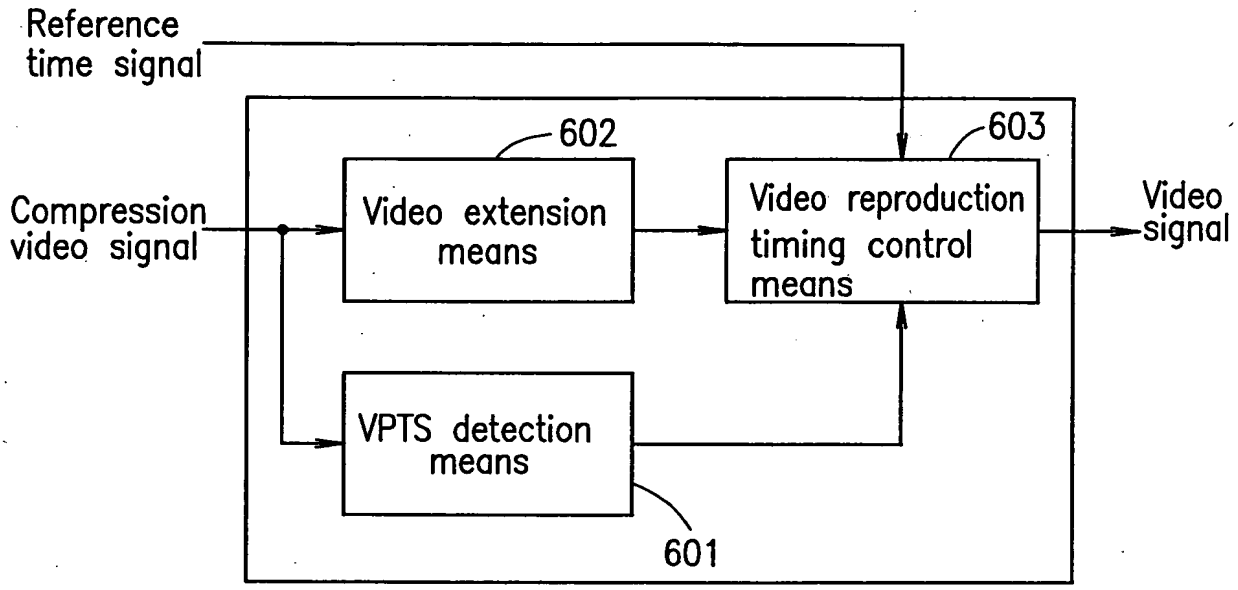

Reference time signal
602
603
Compression video signal
Video extension means
Video reproduction timing control means
Video signal
VPTS detection means
601

FIG.37

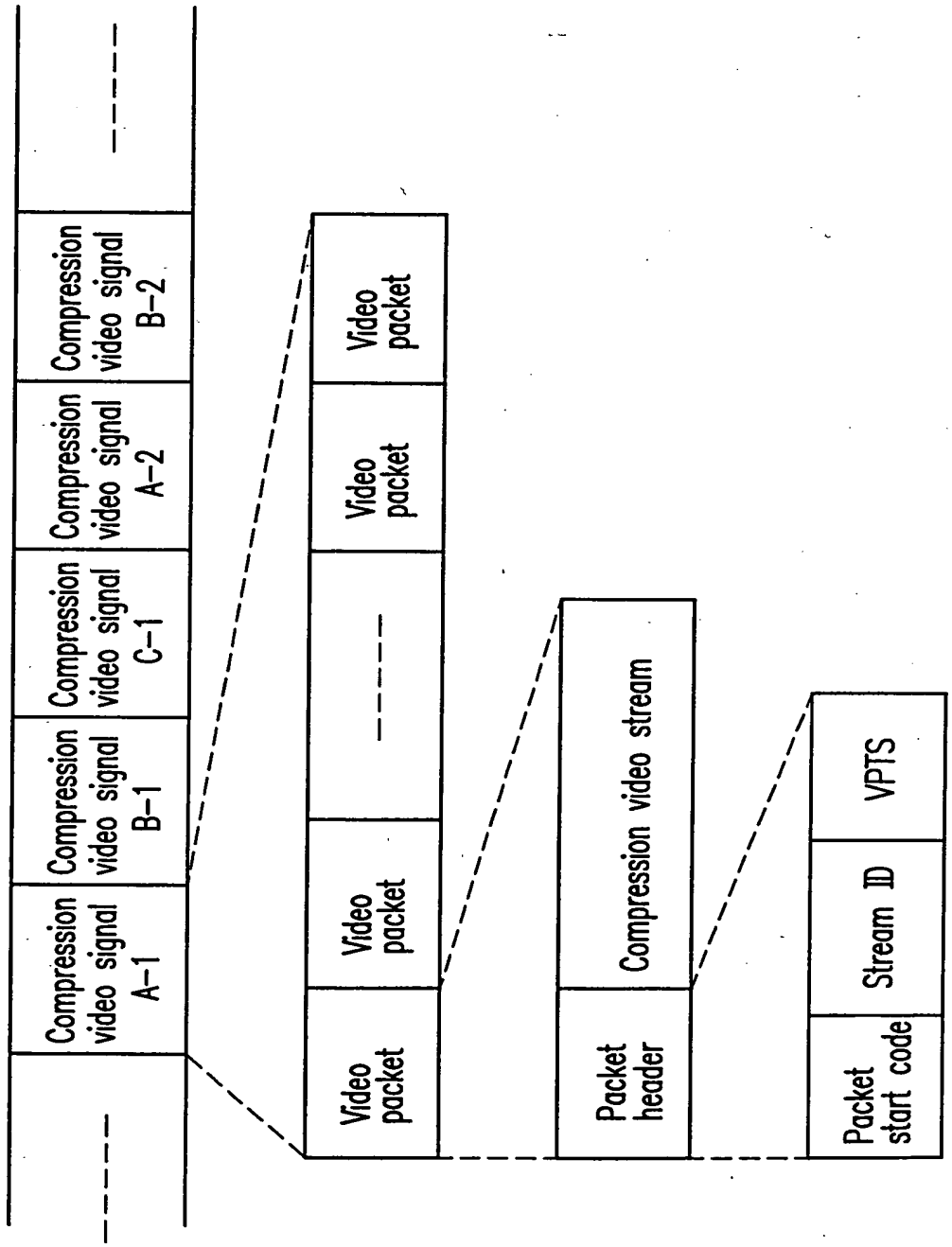
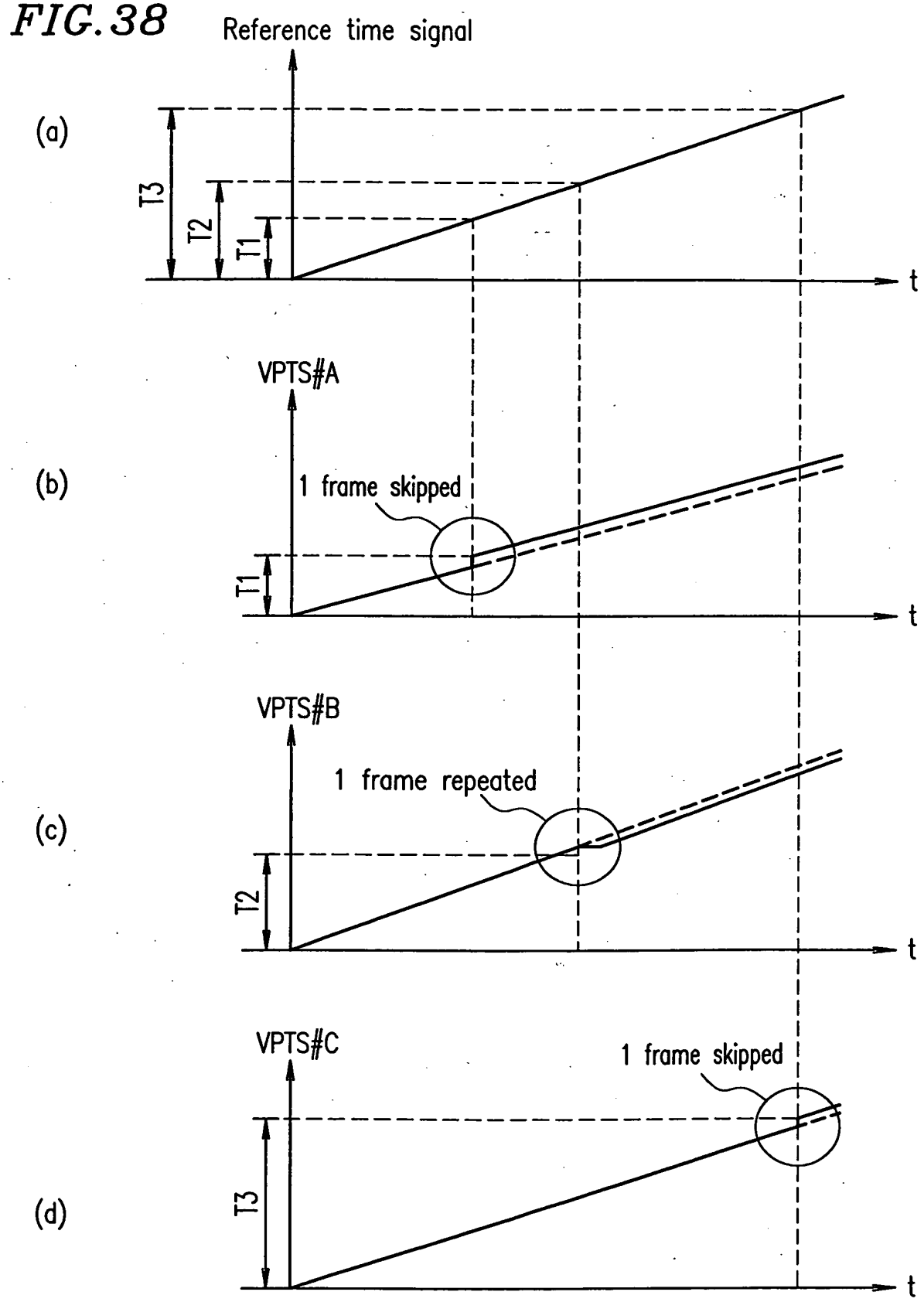

Compression video signal A-1
Compression video signal B-1
Compression video signal C-1
Compression video signal A-2
Compression video signal B-2
Video packet
Video packet
Video packet
Compression video stream
Packet header
Packet start code
Stream ID
VPTS

FIG. 38


Reference time signal
(a)
T3
T2
T1
t
VPTS#A
(b)
1 frame skipped
T1
t
VPTS#B
(c)
1 frame repeated
T2
t
VPTS#C
1 frame skipped
(d)
T3
t

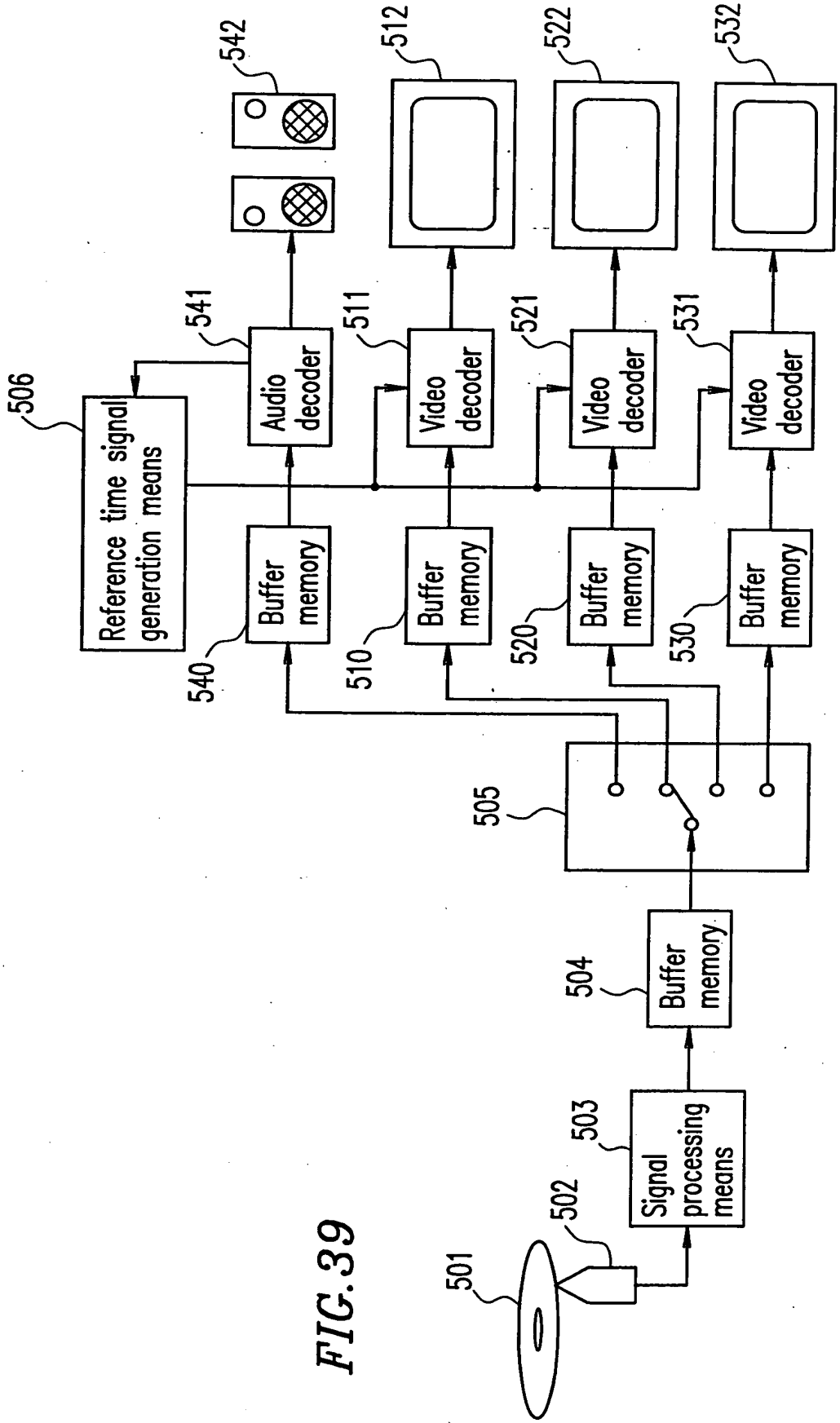

501
502
503
Signal processing means
504
Buffer memory
505
506
Reference time signal generation means
510
Buffer memory
511
Video decoder
512
520
Buffer memory
521
Video decoder
522
530
Buffer memory
531
Video decoder
532
540
Buffer memory
541
Audio decoder
542

FIG. 39

FIG. 40

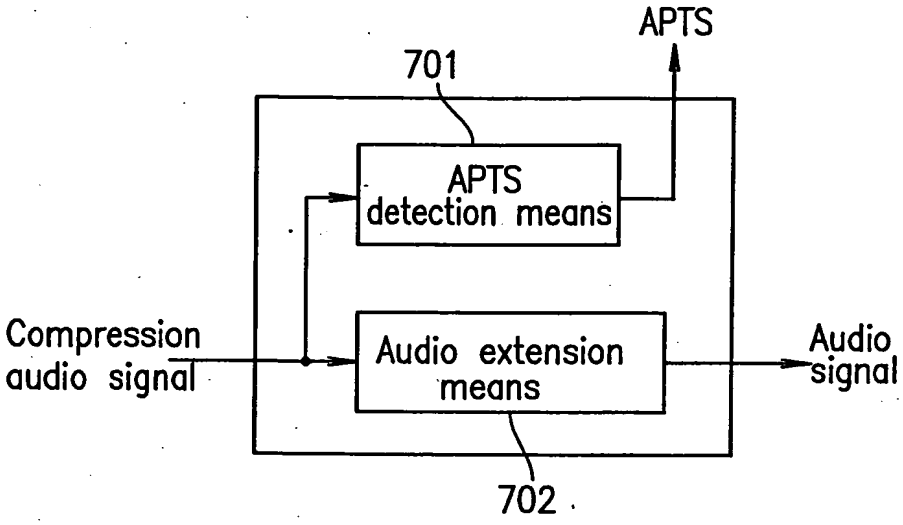

APTS
701
APTS
detection means
Compression
audio signal
Audio extension
means
Audio
signal
702

FIG. 41

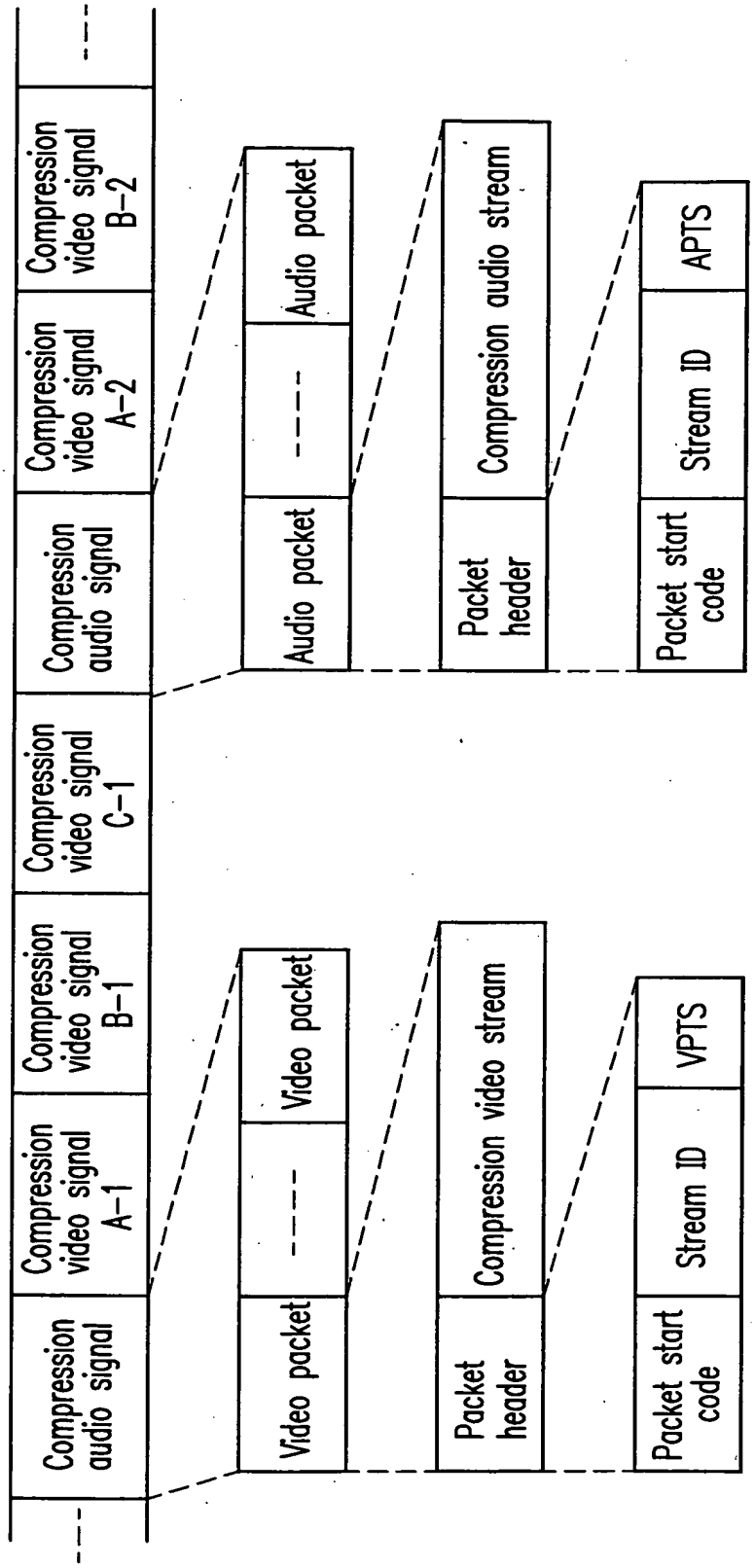
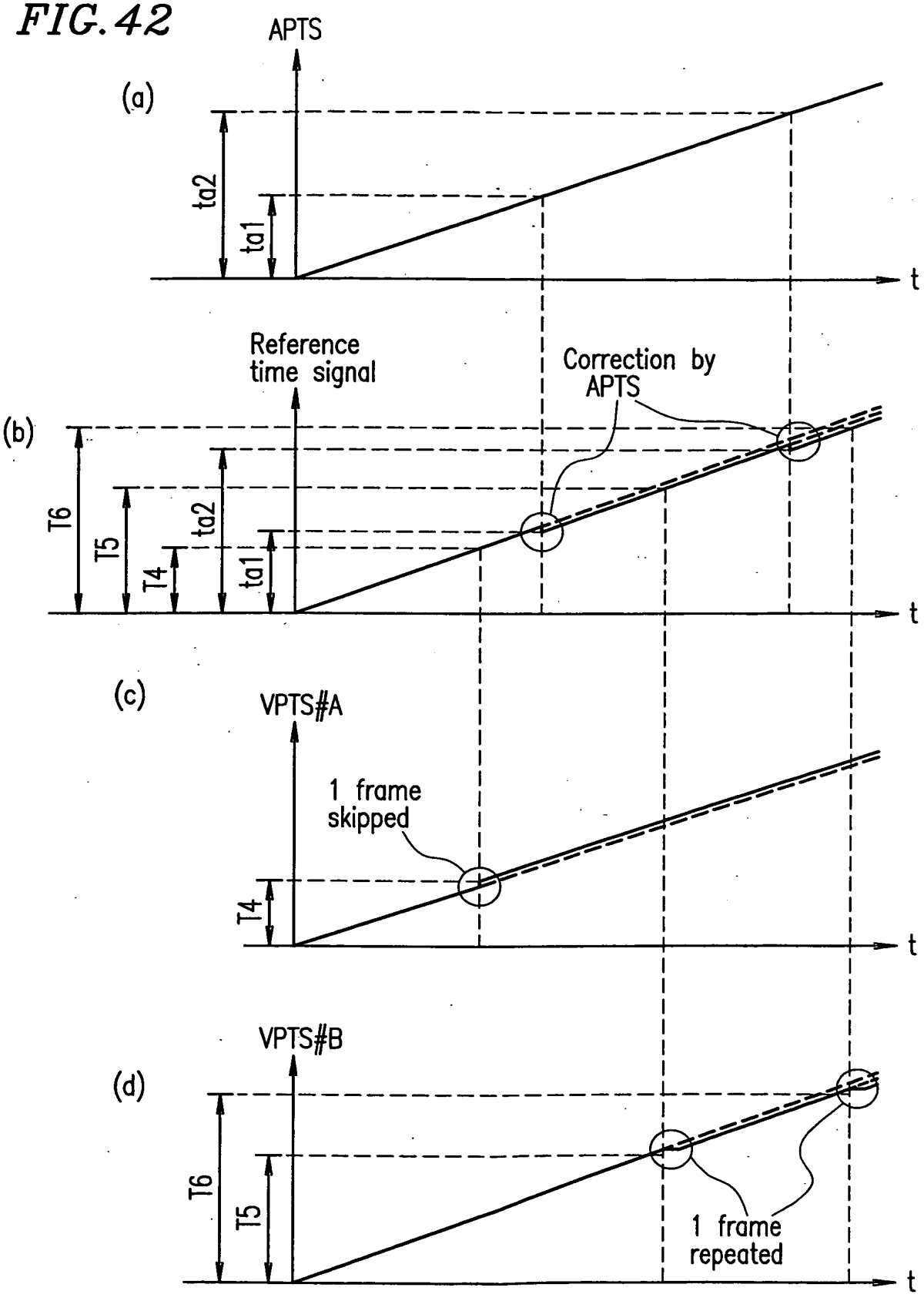

Compression audio signal
Compression video signal A-1
Compression video signal B-1
Compression video signal C-1
Compression audio signal
Compression video signal A-2
Compression video signal B-2
Video packet
Audio packet
Packet header
Compression video stream
Compression audio stream
Packet start code
Stream ID
VPTS
APTS

FIG. 42


APTS
(a)
ta2
ta1
t
Reference time signal
Correction by APTS
(b)
T6
T5
T4
ta2
ta1
t
(c)
VPTS#A
1 frame skipped
T4
t
VPTS#B
(d)
T6
T5
1 frame repeated
t

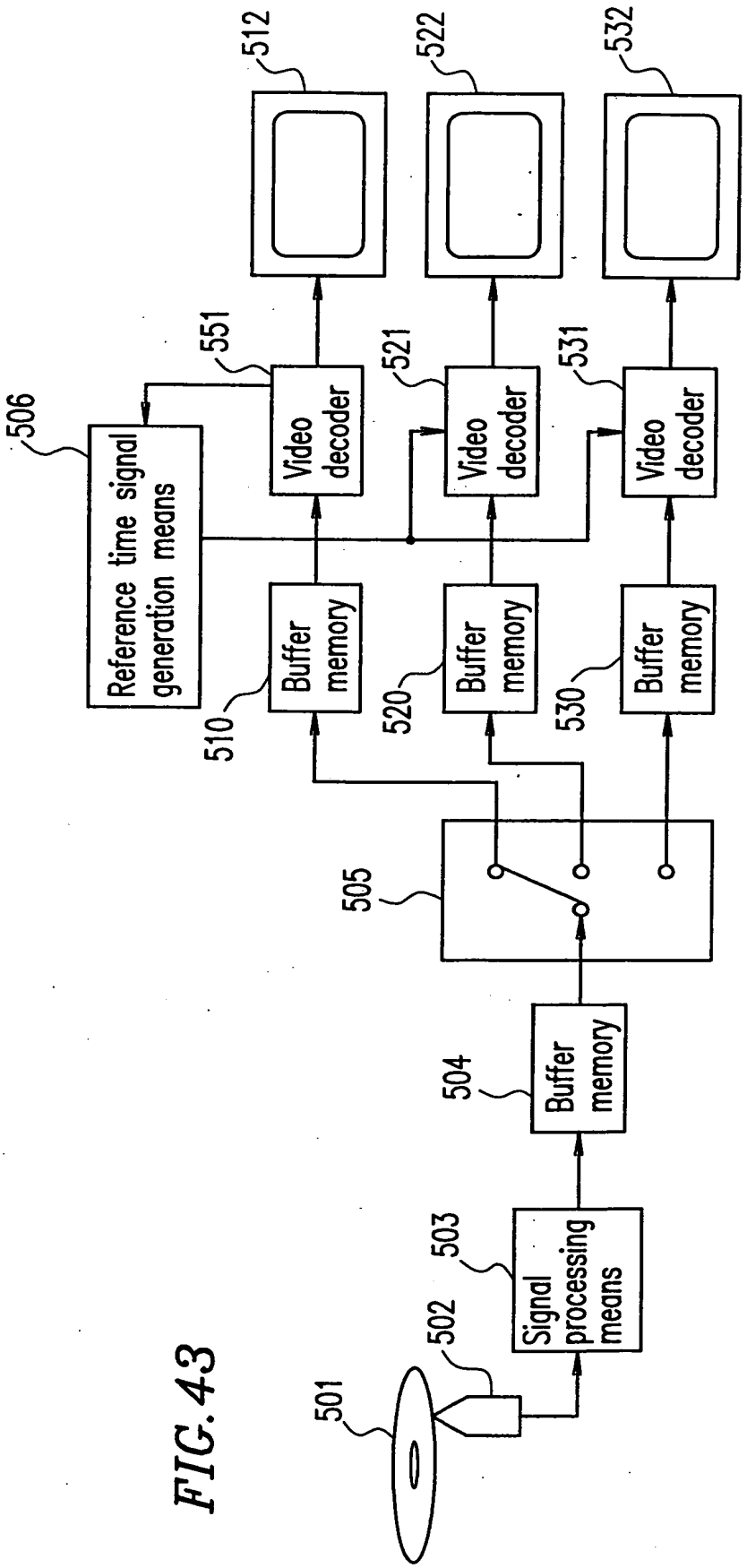

501
502
503
Signal processing means
504
Buffer memory
505
510
520
530
Buffer memory
Buffer memory
Buffer memory
506
Reference time signal generation means
551
521
531
Video decoder
Video decoder
Video decoder
512
522
532

FIG. 43

FIG. 44

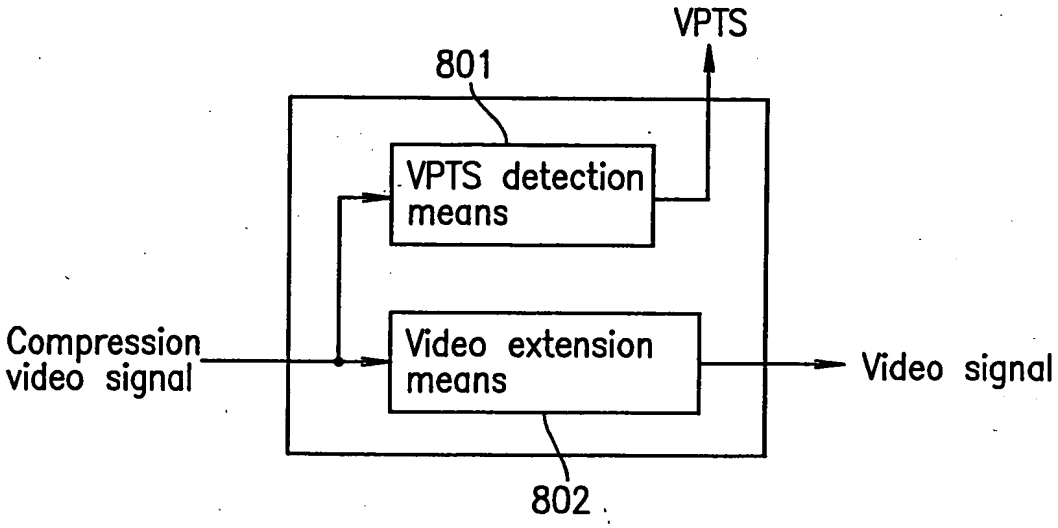
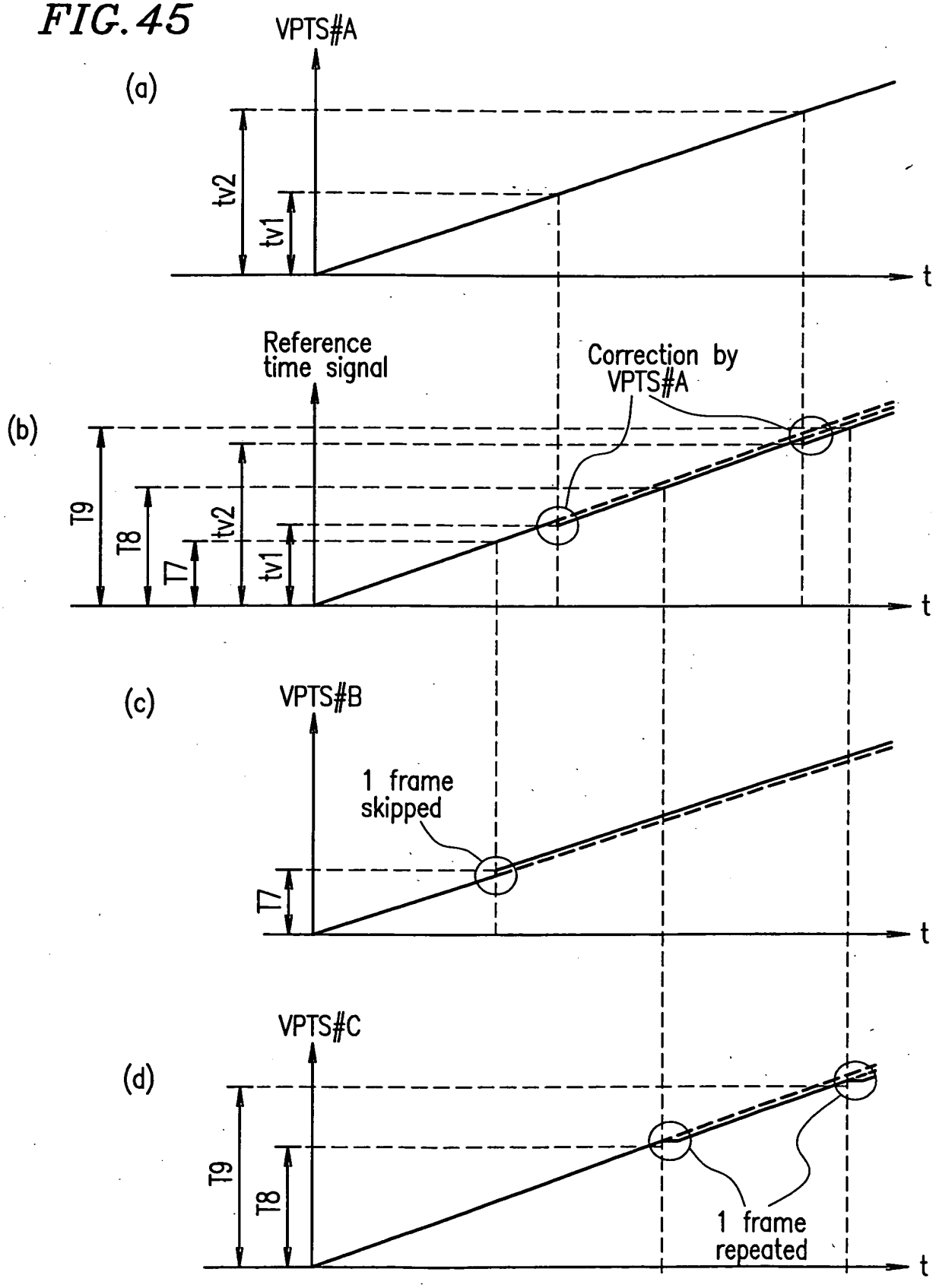

VPTS
801
VPTS detection means
Compression video signal
Video extension means
Video signal
802

FIG. 45


VPTS#A
(a)
tv2
tv1
t
Reference time signal
Correction by VPTS#A
(b)
T9
T8
T7
tv2
tv1
t
VPTS#B
(c)
1 frame skipped
T7
t
VPTS#C
(d)
T9
T8
1 frame repeated
t

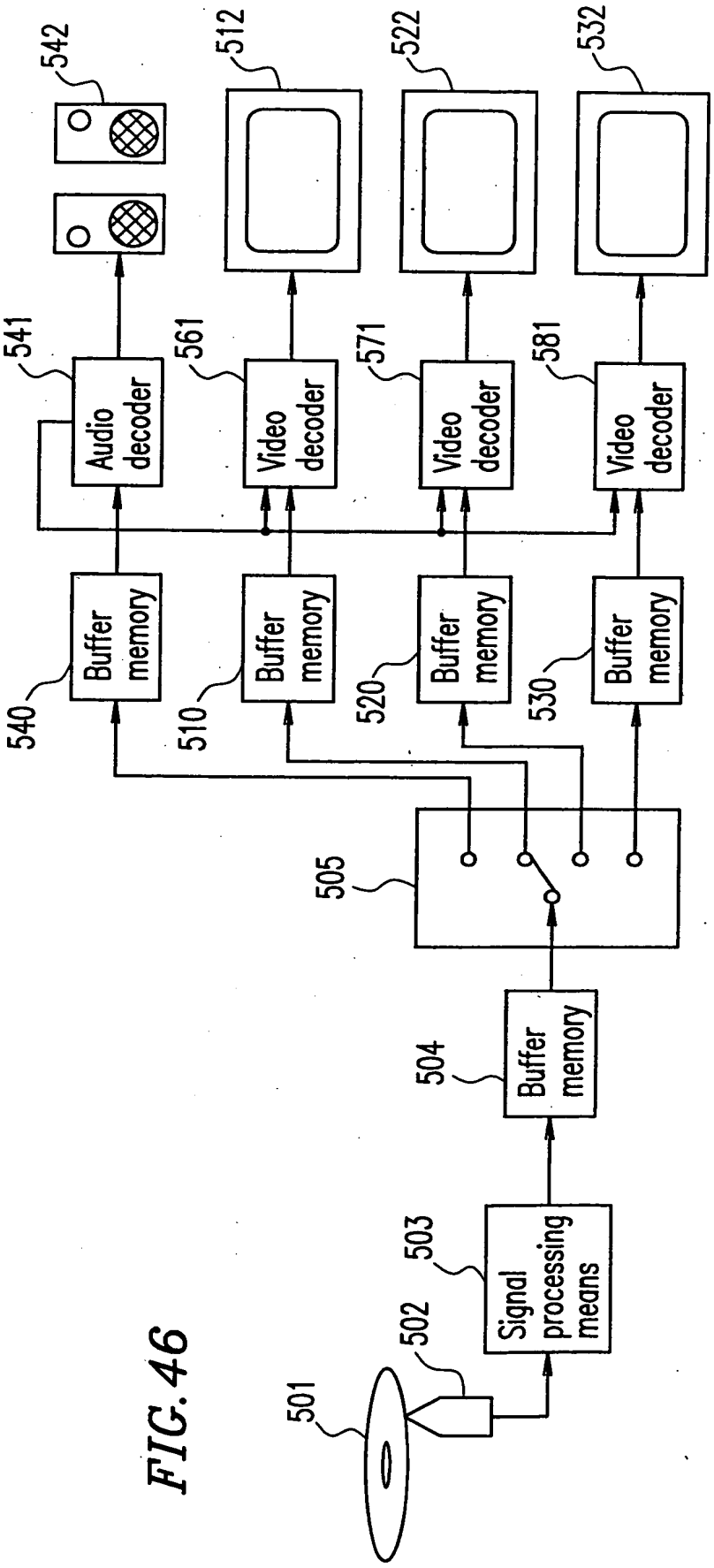

501
502
503
Signal processing means
504
Buffer memory
505
540
Buffer memory
510
Buffer memory
520
Buffer memory
530
Buffer memory
541
Audio decoder
561
Video decoder
571
Video decoder
581
Video decoder
542
512
522
532

FIG. 46

FIG. 47

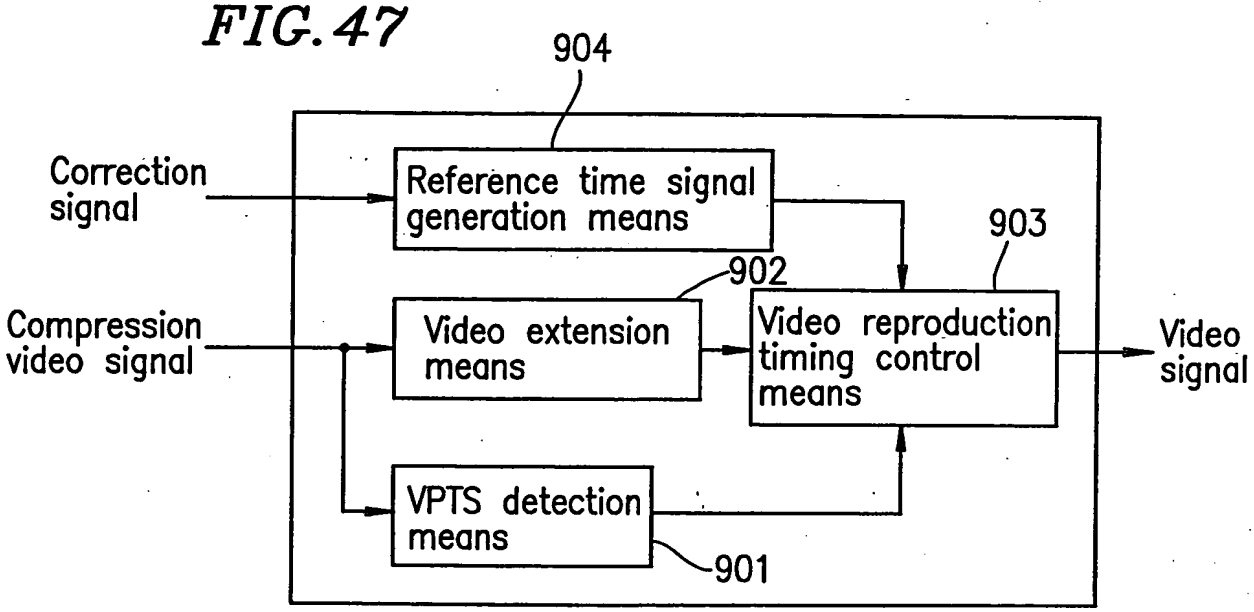

904
Correction signal
Reference time signal generation means
903
902
Compression video signal
Video extension means
Video reproduction timing control means
Video signal
VPTS detection means
901

FIG. 48

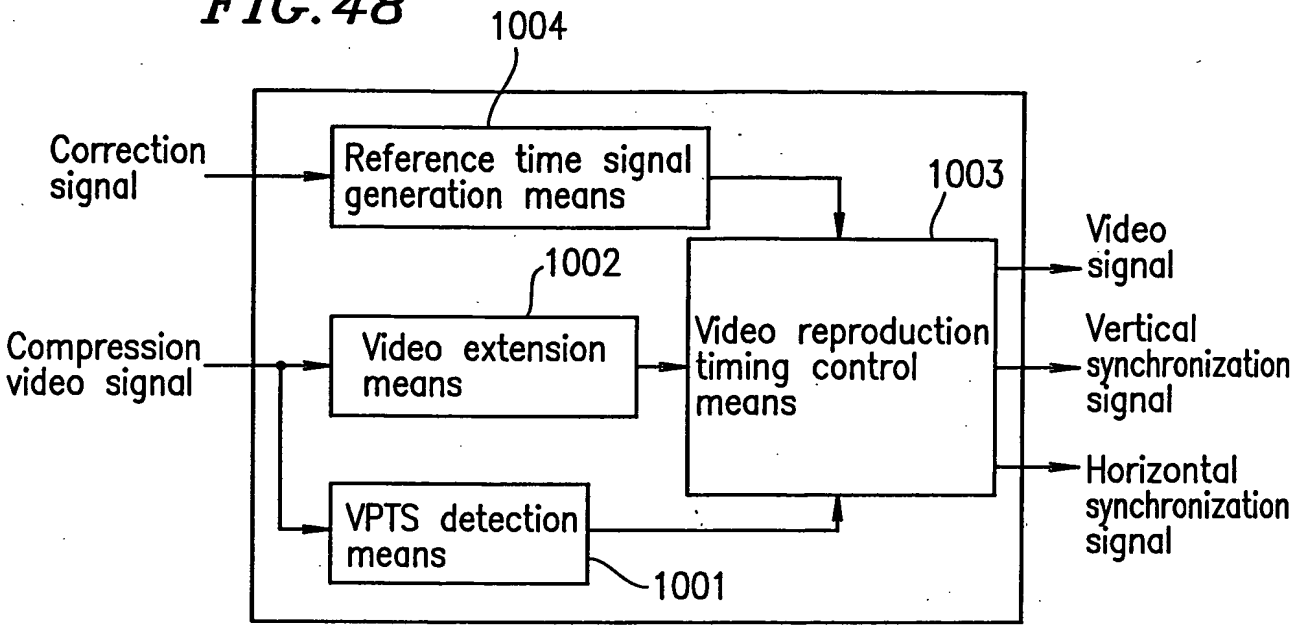
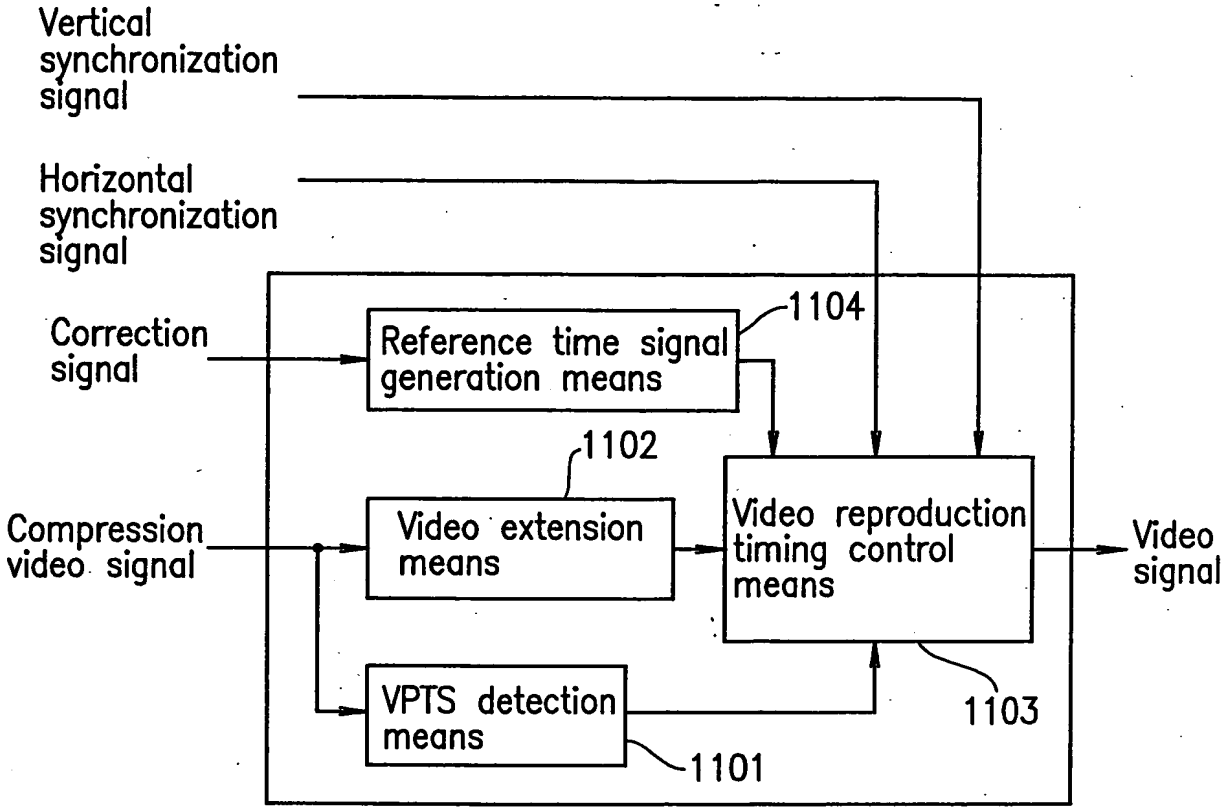

1004
Correction signal
Reference time signal generation means
1003
Video signal
1002
Compression video signal
Video extension means
Video reproduction timing control means
Vertical synchronization signal
Horizontal synchronization signal
VPTS detection means
1001

FIG. 49


Vertical synchronization signal
Horizontal synchronization signal
Correction signal
Reference time signal generation means
1104
1102
Compression video signal
Video extension means
Video reproduction timing control means
Video signal
VPTS detection means
1103
1101

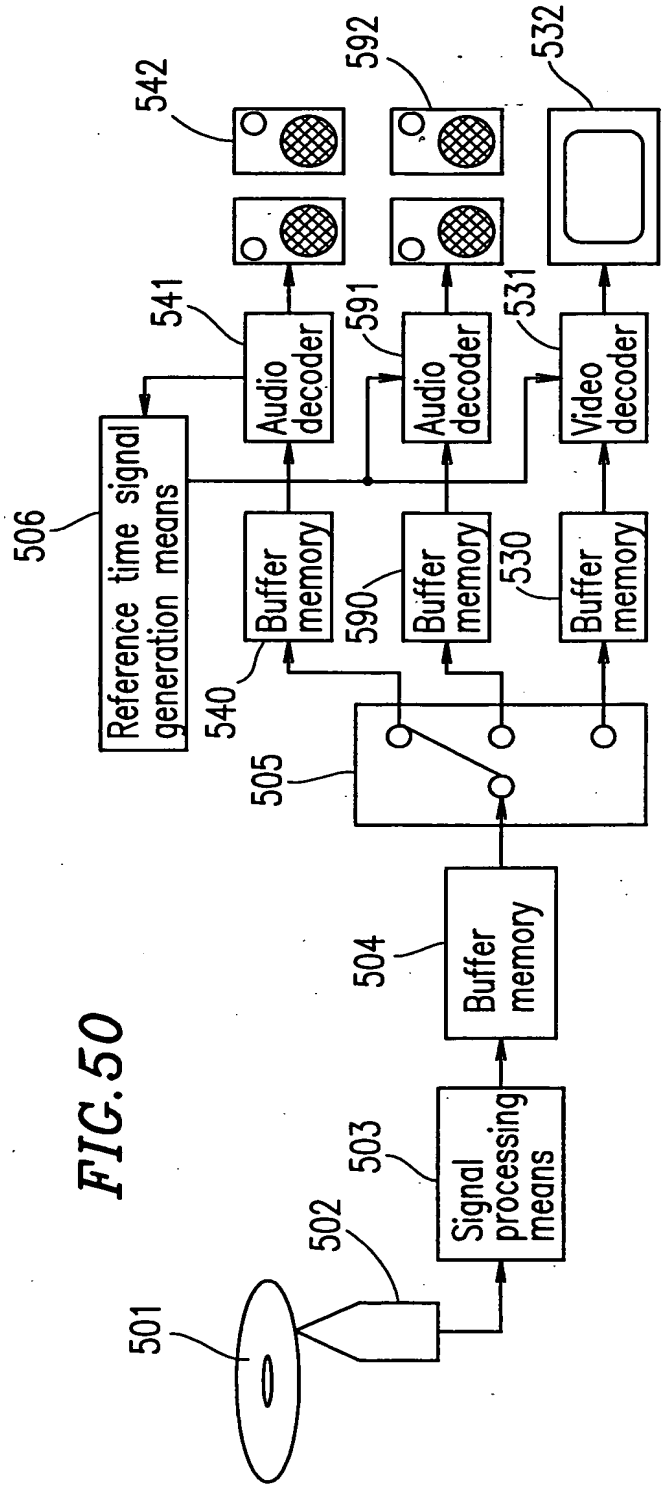


FIG. 50

FIG.51

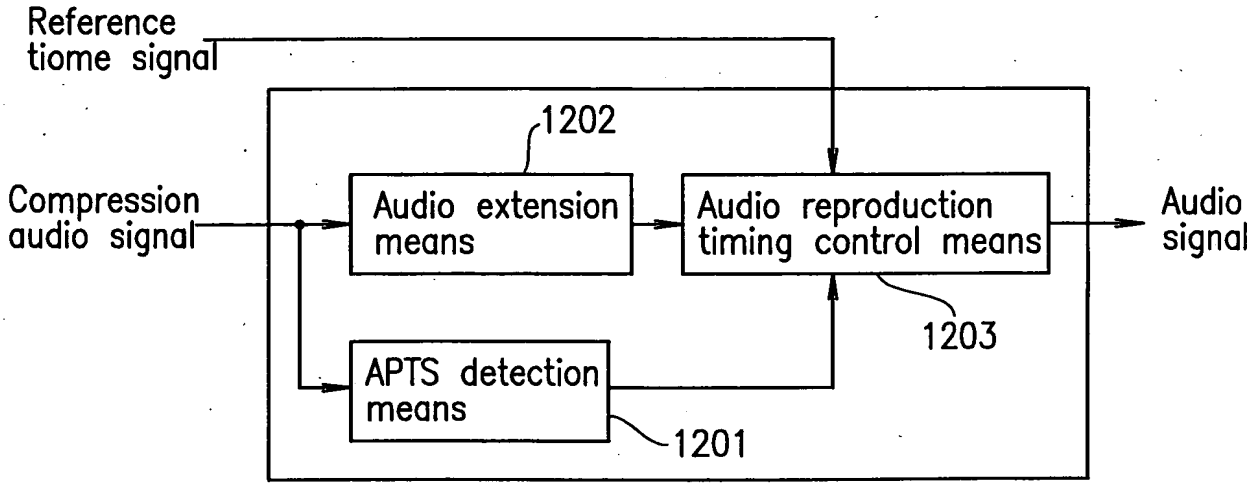

Reference
tiome signal
1202
Compression
audio signal
Audio extension
means
Audio reproduction
timing control means
Audio
signal
1203
APTS detection
means
1201

FIG. 52

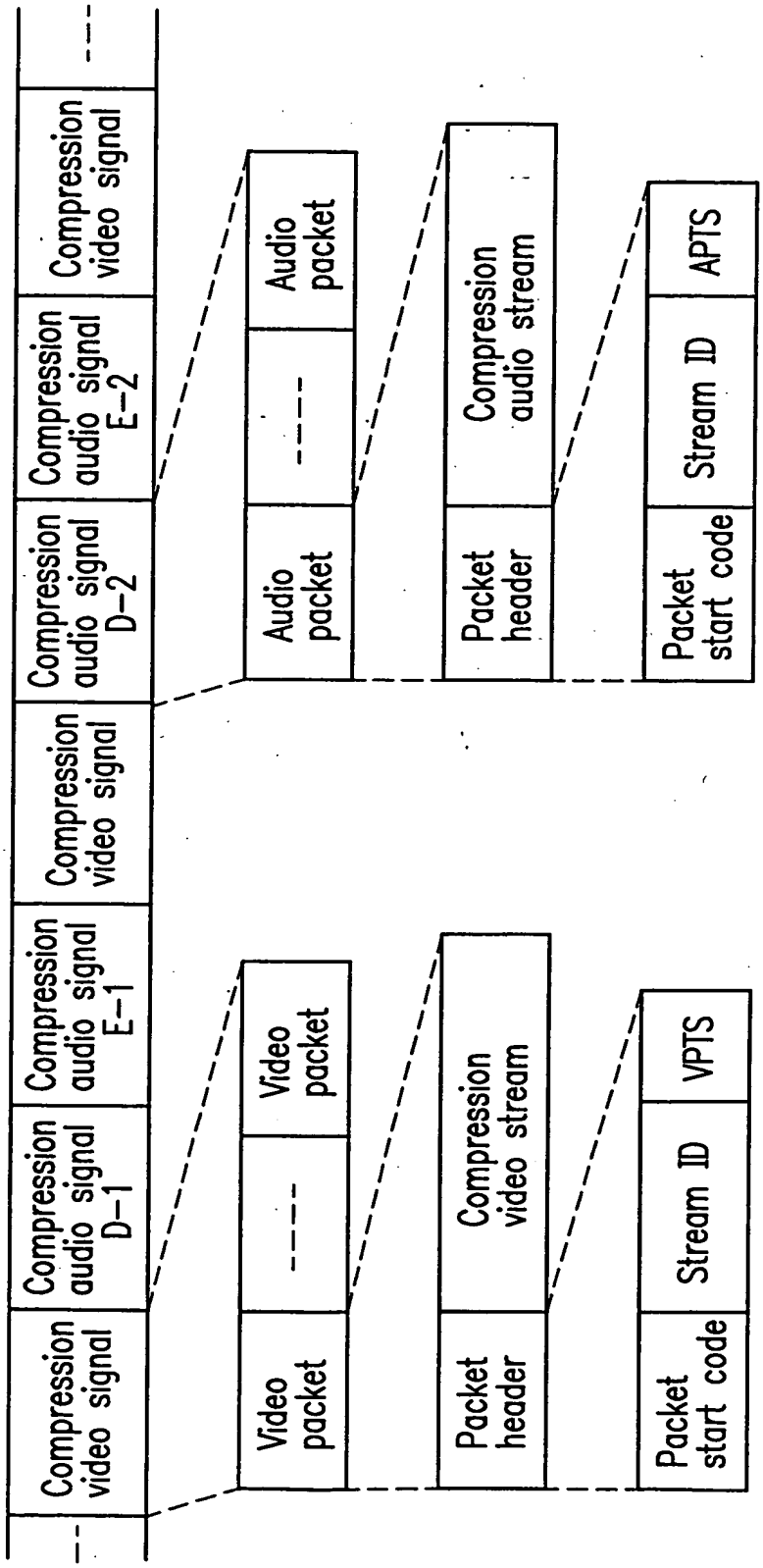

Compression video signal
Compression audio signal D-1
Compression audio signal E-1
Compression video signal
Compression audio signal D-2
Compression audio signal E-2
Compression video signal
Video packet
Video packet
Audio packet
Audio packet
Packet header
Compression video stream
Packet header
Compression audio stream
Packet start code
Stream ID
VPTS
Packet start code
Stream ID
APTS

FIG. 53

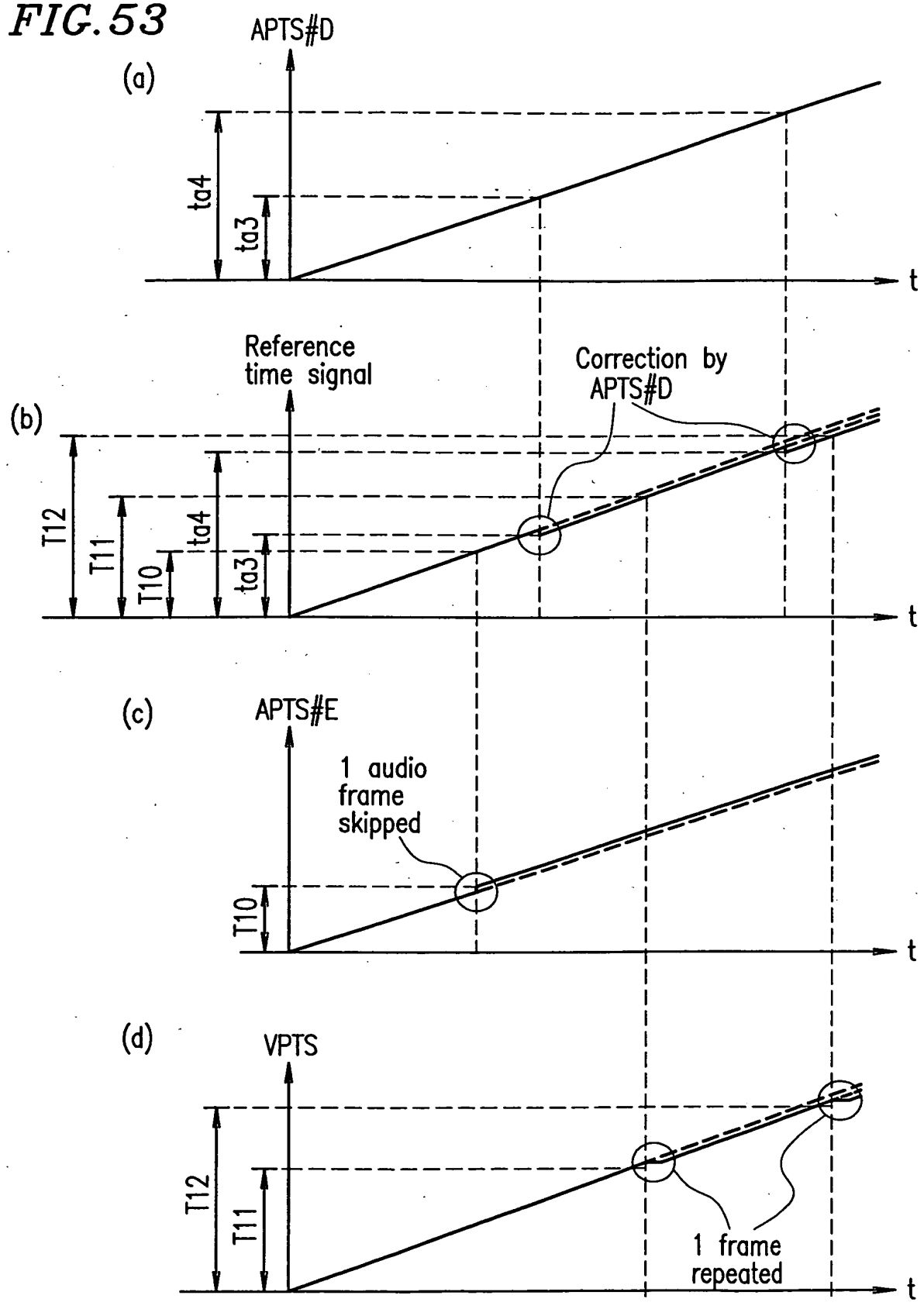

APTS#D
(a)
ta4
ta3
t
Reference time signal
Correction by APTS#D
(b)
T12
T11
T10
ta4
ta3
t
(c)
APTS#E
1 audio frame skipped
T10
t
(d)
VPTS
T12
T11
1 frame repeated
t

FIG.54

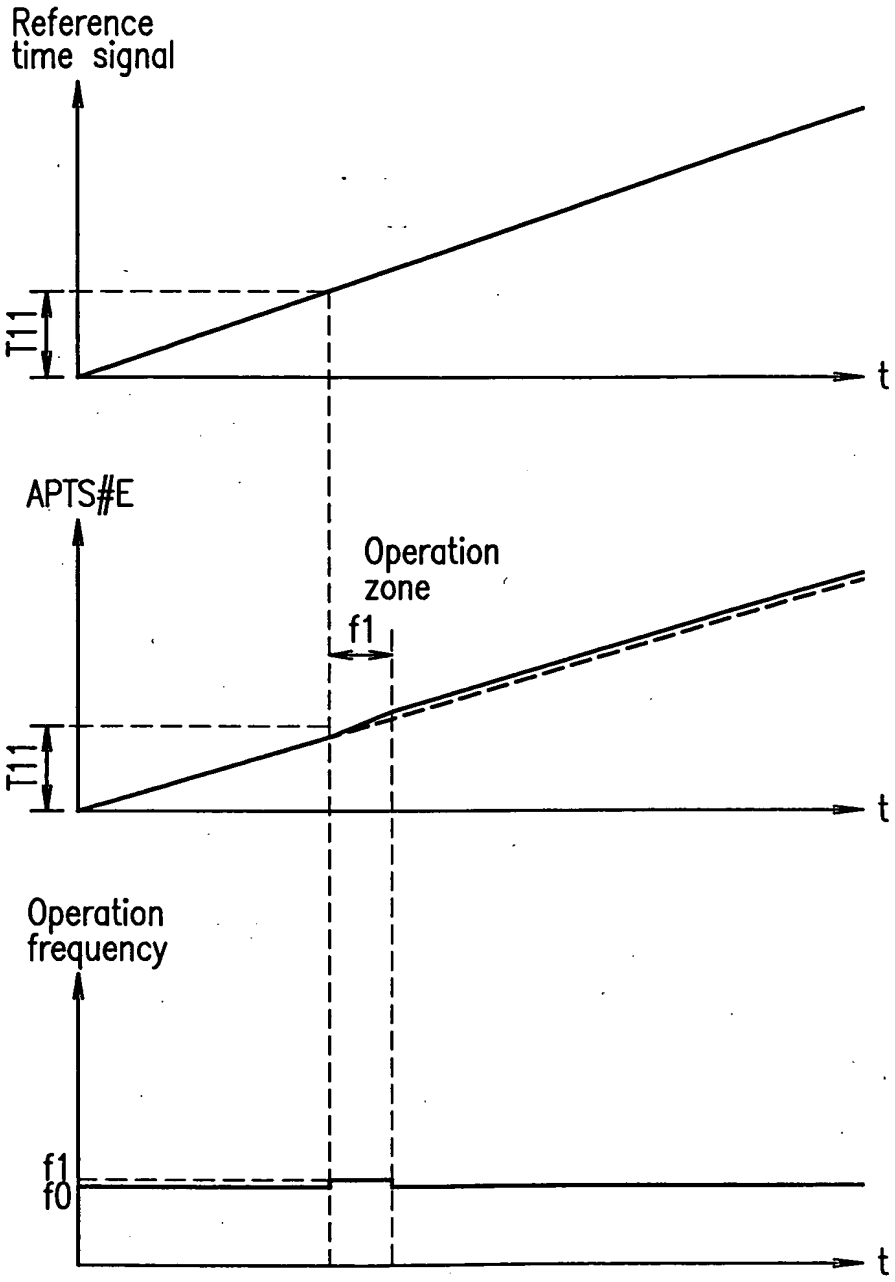
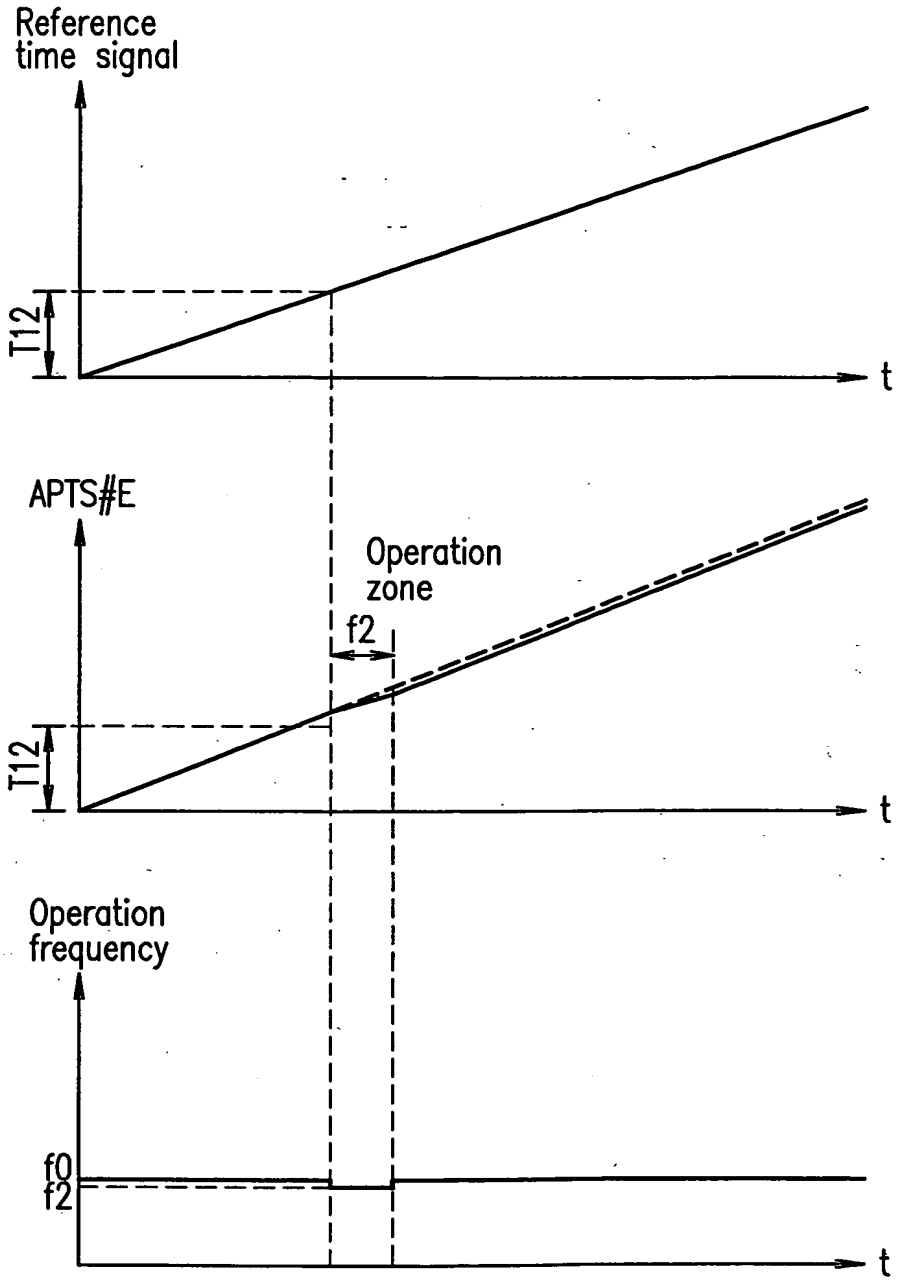

(a)
Reference time signal
T11
t
(b)
APTS#E
Operation zone
f1
T11
t
(c)
Operation frequency
f1
f0
t

FIG. 55


(a)
Reference time signal
T12
t
(b)
APTS#E
Operation zone
f2
T12
t
(c)
Operation frequency
f0
f2
t

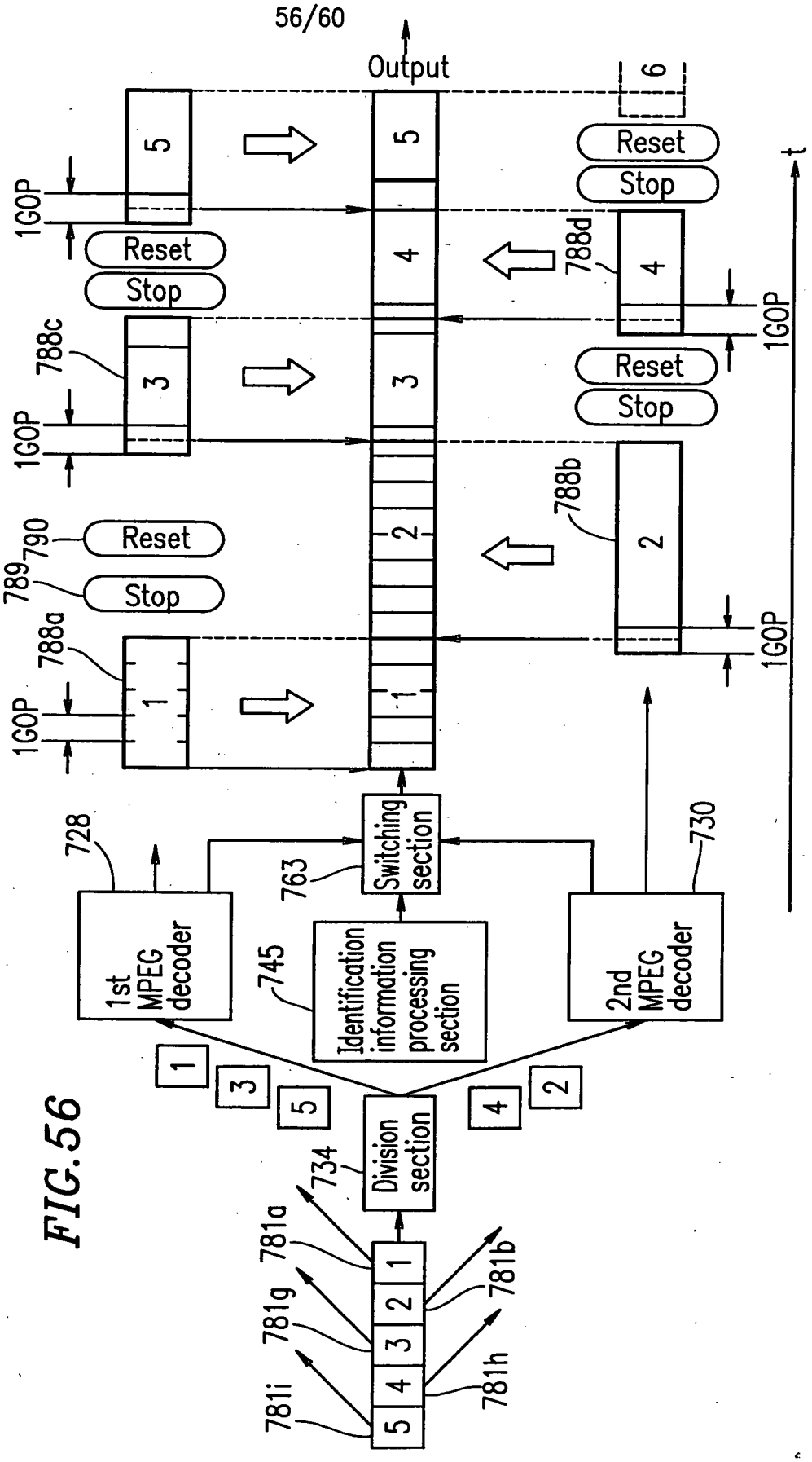
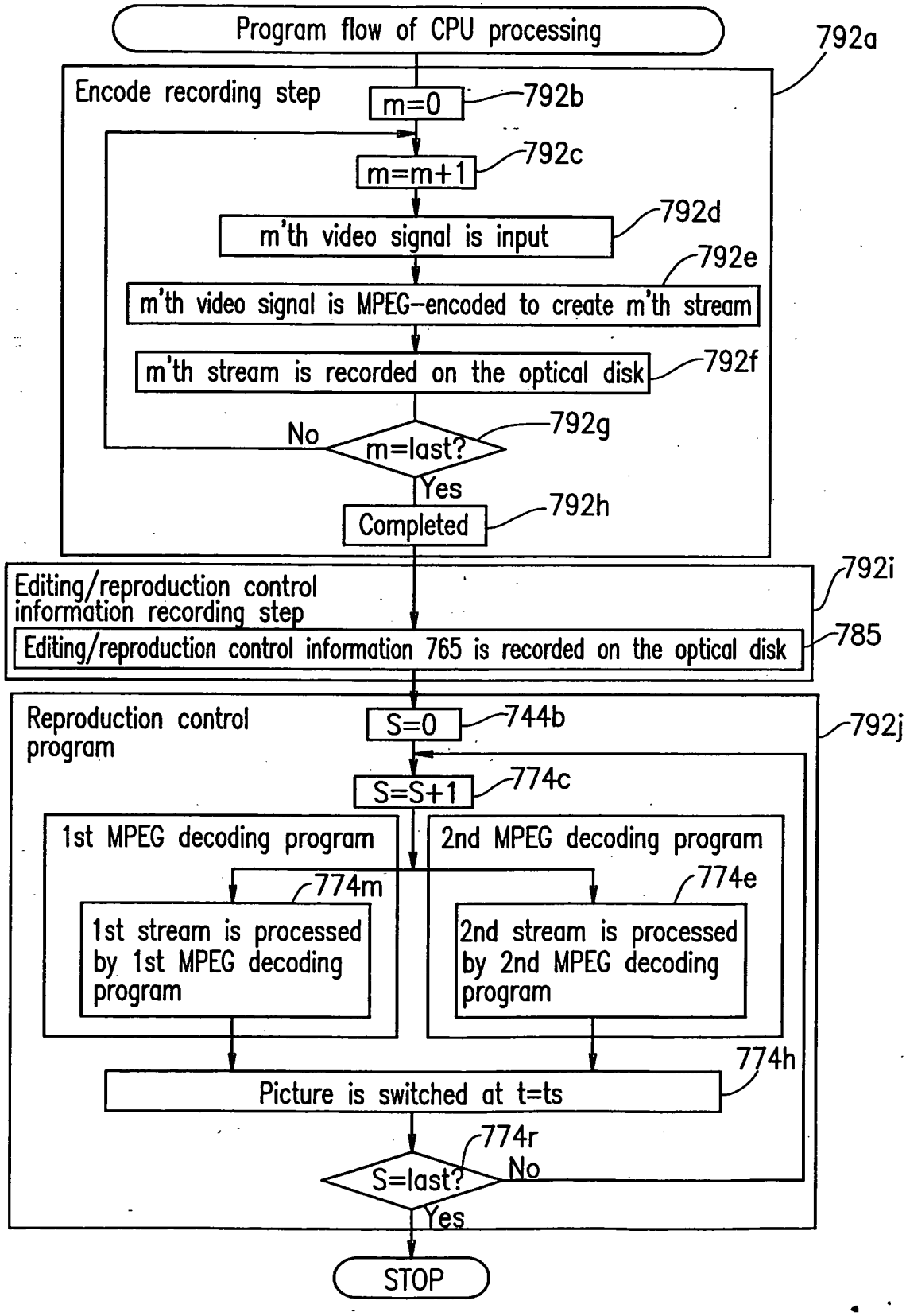

Output
t
1GOP
Reset
Stop
788a
788b
788c
788d
789
790
Switching section
763
728
730
1st MPEG decoder
2nd MPEG decoder
745
Identification information processing section
Division section
734
781a
781b
781g
781h
781i

FIG.56

FIG. 57


Program flow of CPU processing
792a
Encode recording step
m=0
792b
m=m+1
792c
m'th video signal is input
792d
m'th video signal is MPEG-encoded to create m'th stream
792e
m'th stream is recorded on the optical disk
792f
No
m=last?
792g
Yes
Completed
792h
Editing/reproduction control information recording step
792i
Editing/reproduction control information 765 is recorded on the optical disk
785
Reproduction control program
S=0
744b
792j
S=S+1
774c
1st MPEG decoding program
2nd MPEG decoding program
774m
774e
1st stream is processed by 1st MPEG decoding program
2nd stream is processed by 2nd MPEG decoding program
774h
Picture is switched at t=ts
774r
S=last?
No
Yes
STOP

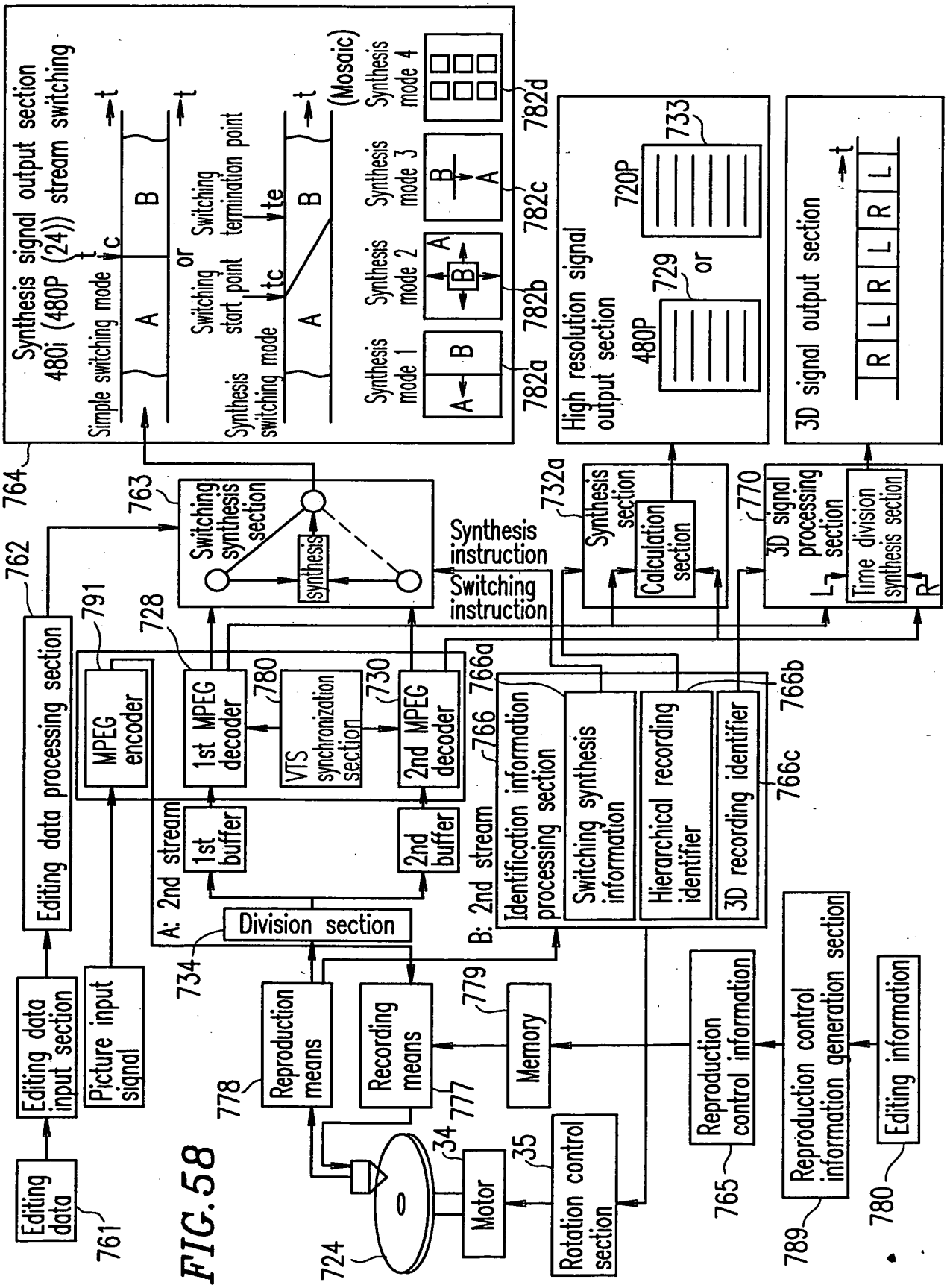

Synthesis signal output section
480i (480P (24)) stream switching
Simple switching mode
Switching start point
Switching termination point
Synthesis switching mode
Synthesis mode 1
Synthesis mode 2
Synthesis mode 3
Synthesis mode 4
(Mosaic)
764
763
Switching synthesis section
synthesis
762
791
728
MPEG encoder
1st MPEG decoder
780
VTS synchronization section
730
2nd MPEG decoder
Editing data processing section
A: 2nd stream
1st buffer
2nd buffer
B: 2nd stream
Division section
734
Identification information processing section
766
766a
766b
766c
Switching synthesis information
Hierarchical recording identifier
3D recording identifier
Synthesis instruction
Switching instruction
732a
Synthesis section
Calculation section
770
3D signal processing section
Time division synthesis section
High resolution signal output section
720P
733
480P
729
or
3D signal output section
R L R L R L
Editing data input section
Picture input signal
Editing data
761
778
Reproduction means
Recording means
777
779
Memory
34
35
Motor
Rotation control section
724
765
Reproduction control information
789
Reproduction control information generation section
780
Editing information

FIG. 58

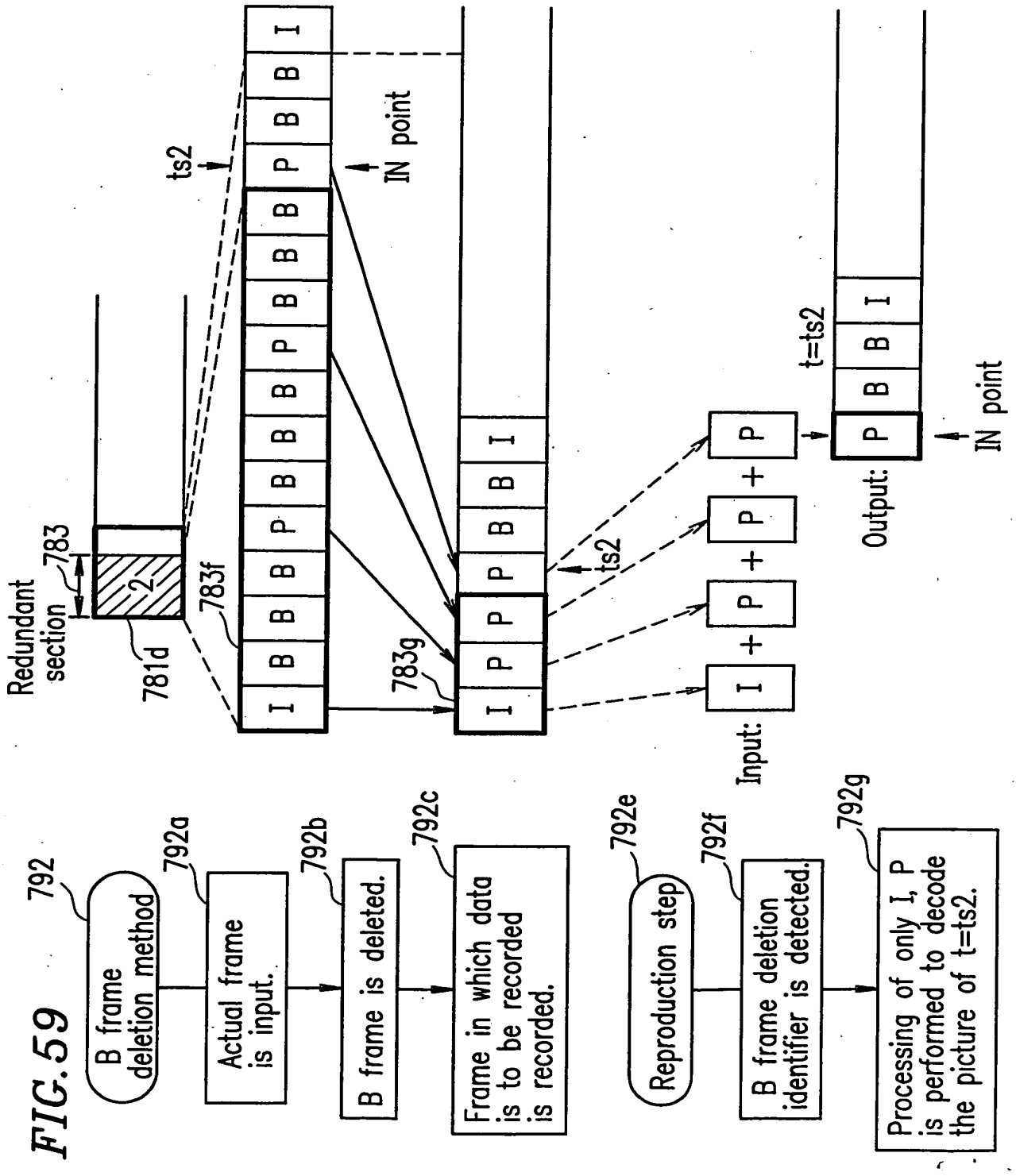

792
B frame deletion method
792a
Actual frame is input.
792b
B frame is deleted.
792c
Frame in which data is to be recorded is recorded.
792e
Reproduction step
792f
B frame deletion identifier is detected.
792g
Processing of only I, P is performed to decode the picture of t=ts2.
Redundant section
783
781d
783f
783g
ts2
IN point
Input:
Output:
t=ts2
IN point

FIG. 59

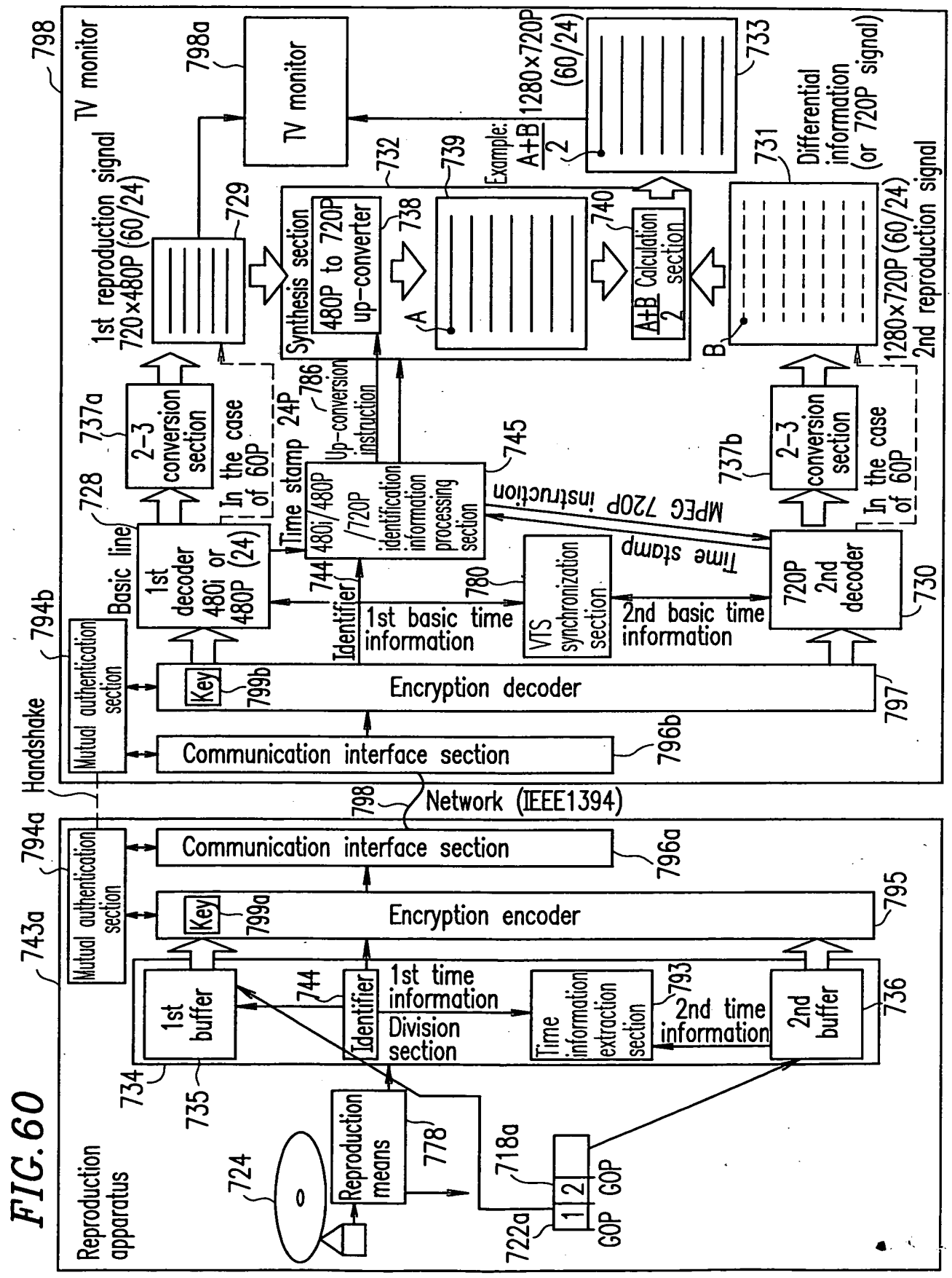

Reproduction apparatus
724
Reproduction means
778
718a
722a
GOP
743a
734
735
1st buffer
744
Identifier
1st time information
Division section
Time information extraction section
793
2nd time information
2nd buffer
736
795
Encryption encoder
Key
799a
Mutual authentication section
794a
Communication interface section
796a
Network (IEEE1394)
798
Handshake
794b
Mutual authentication section
Key
799b
Encryption decoder
797
Communication interface section
796b
Basic line
1st decoder 480i or 480P (24)
728
744
Identifier
1st basic time information
780
VTS synchronization section
2nd basic time information
720P 2nd decoder
730
Time stamp
MPEG 720P instruction
480i/480P /720P identification information processing section
745
Up-conversion instruction
786
Time stamp 24P
In the case of 60P
2-3 conversion section
737a
737b
1st reproduction signal 720×480P (60/24)
729
Synthesis section
480P to 720P up-converter
732
738
A
740
A+B 2 Calculation section
B
731
Differential information (or 720P signal)
1280×720P (60/24)
2nd reproduction signal
Example: A+B/2
1280×720P (60/24)
733
798a
TV monitor
798
TV monitor

FIG. 60